

Motivation

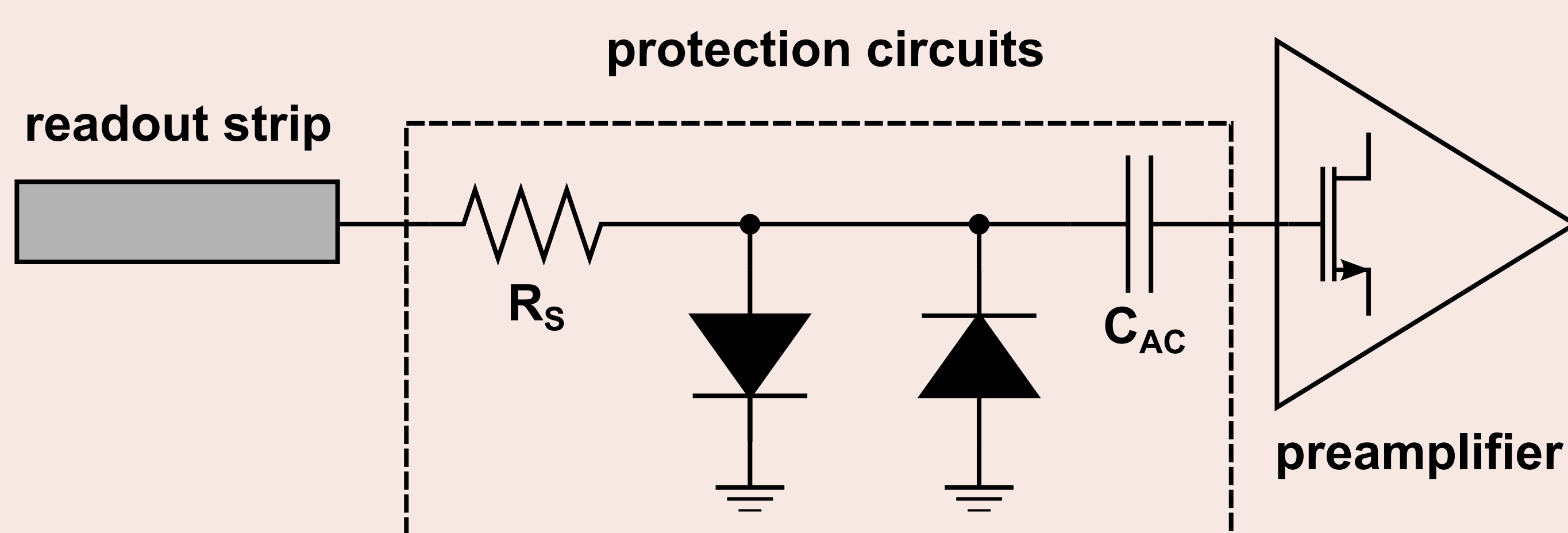
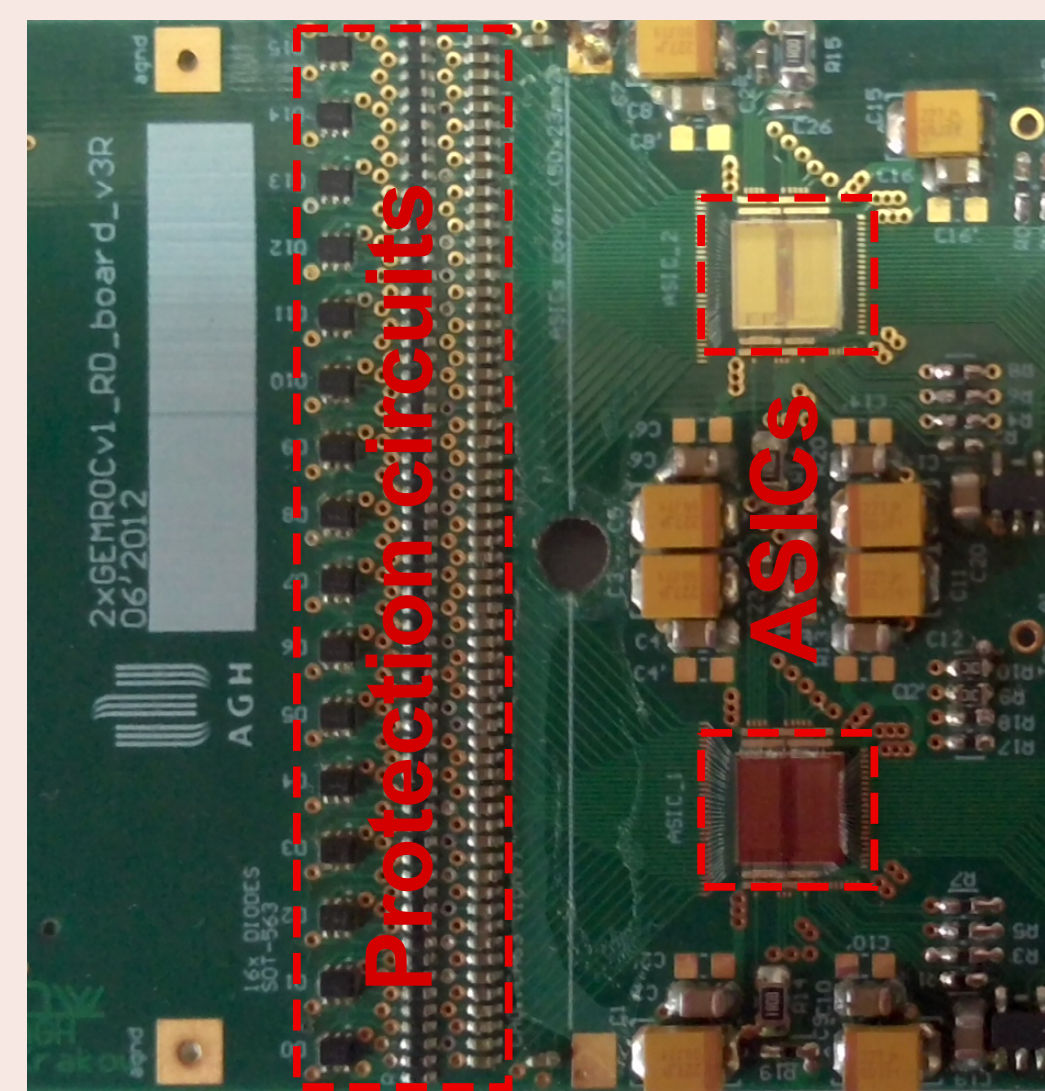
One of the major problems that have to be addressed in the design of the front-end electronics for readout of MPGDs is its immunity against possible random discharges inside active detector volume. A commonly used solution to this problem is an input protection circuit built of discrete Surface Mount Device (SMD) components. Such a solution has, however, several drawbacks, including large area occupied by the SMD components and associated stray capacitance at the input, necessity of using advanced and expensive Printed Circuit Board (PCB) technologies, demanding assembly techniques, and high cost of the SMD components themselves. These issues become particularly critical for systems with high channel counts and high density readout employing the front-end electronics built as multichannel ASICs implemented in modern CMOS technologies. With continuous downscaling of the CMOS technologies the breakdown voltages of transistors are becoming lower and lower and for any CMOS device input protection is needed to prevent damages during handling and assembling of such devices. Therefore, the problem of Electro Static Discharge (ESD) is being continuously investigated in the field of CMOS integrated circuits. The vendors of the CMOS technologies deliver recommended ESD protection circuits, which are qualified according to the standards used in the electronics industry. Within these standards the voltages vary in the range from 2kV to 10kV. Although the voltages are comparable with the voltages used for biasing the MPGDs the equivalent electrical circuit of a MPGD is different compared to the circuit used in the ESD protection. First of all, in case of a discharge occurring in the MPGD the resistance of the discharging path is much lower. Thus, a protection circuits against discharges in MPGDs have to handle much higher currents and the typical circuits recommended for protection against ESD are not adequate at all. On the other hand, immunity of the front-end circuit against sparks occurring in MPGDs depends on the design of the front-end circuit itself, in particular on its input impedance. Therefore, the input protection circuit should be tuned specifically for a given type of MPGD and given design of the input stage if one wants to minimize additional capacitance and resistance at the input, which will affect the noise performance of the system.

We demonstrated before [1] that integrated input protection could be quite robust against discharges expected in MPGDs. However, the prototype circuit was designed using a conservative approach resulting in large input capacitance. In this work we present test results of newly designed input protection structures. These structures have been designed using smaller devices resulting in smaller input capacitance. In addition, structures with series resistors have been implemented, which allow us to evaluate the trade-off between the input capacitance and the series resistance introduced by the protection circuits from the noise minimizing point of view. The ASIC was manufactured in the 350nm CMOS process.

[1] T.Fiutowski, W. Dąbrowski, S. Koperny, P. Wiącek, *Front-end electronics for Micro Pattern Gas Detector with integrated input protection against discharges*, 2016 JINST 11 C01036.

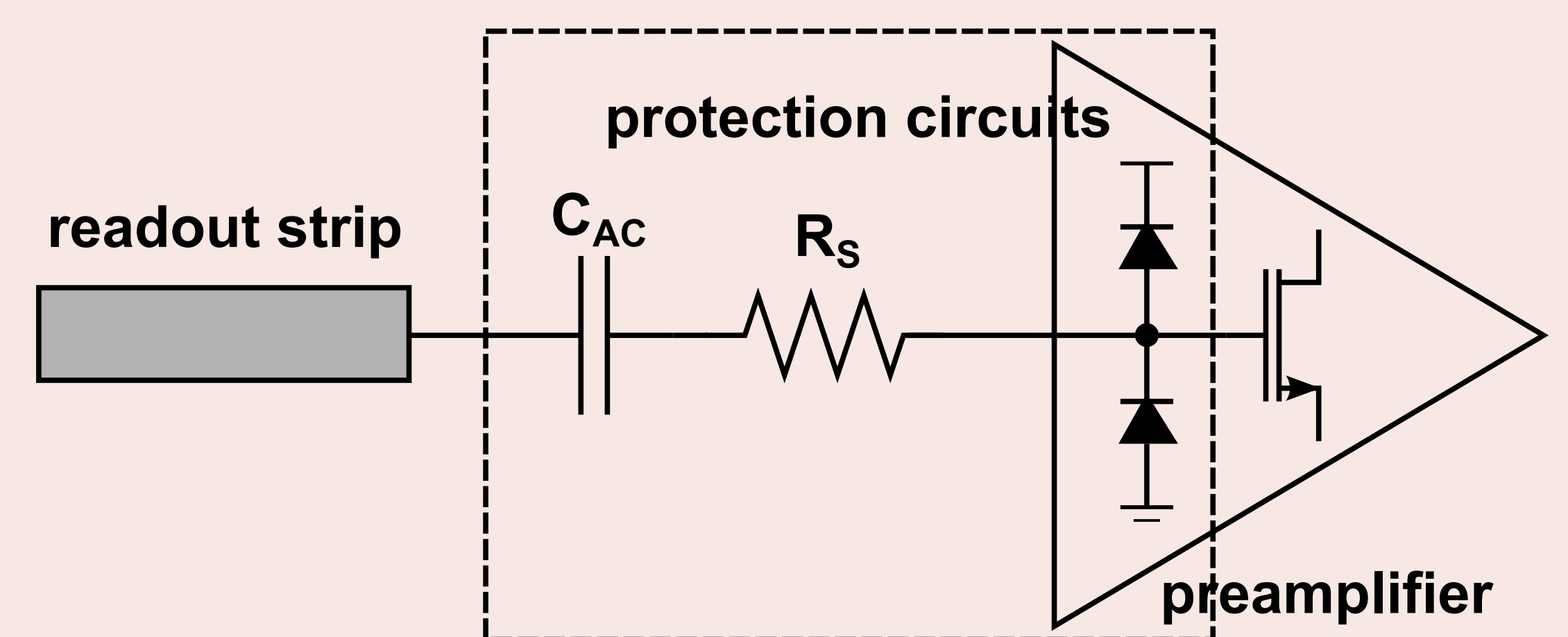
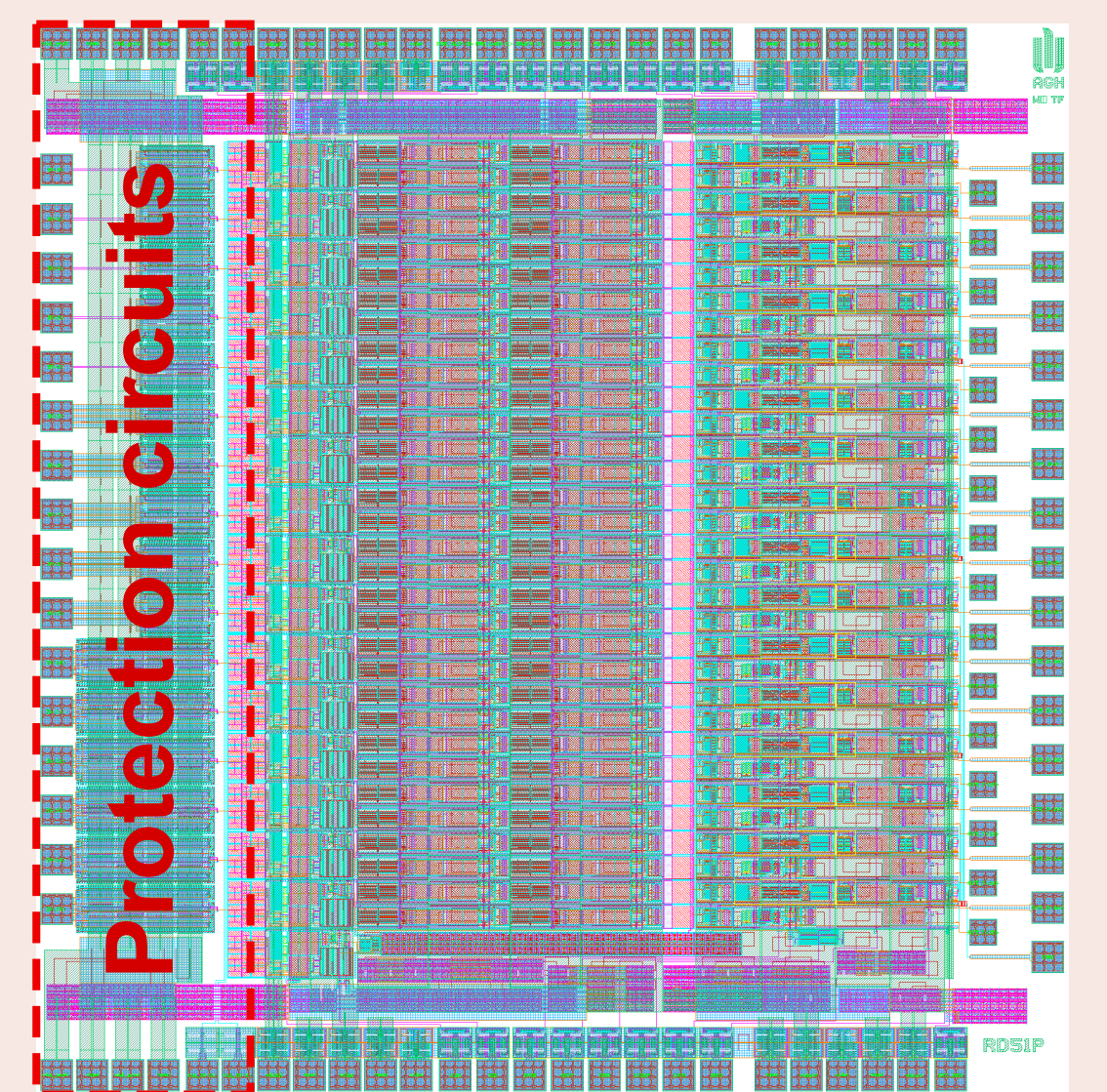
Protection circuits build of SMD components

- Large area occupied by the SMD components (7 mm × 42 mm for 64 channel readout).
- Additional stray capacitance.
- Advanced and expensive PCB technology.
- Demanding assembly techniques.
- High cost of elements.



Integrated protection circuits

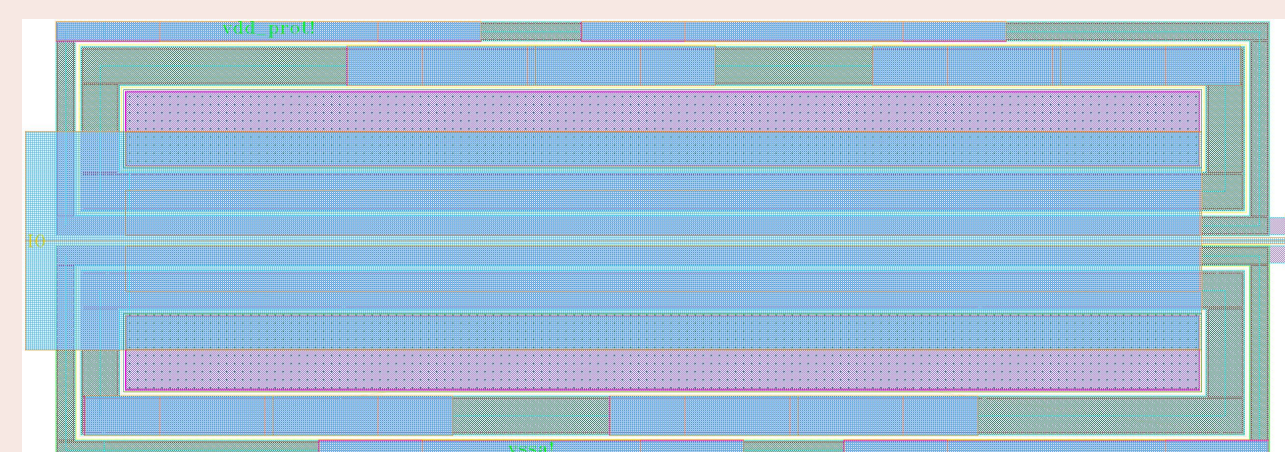
- Small area (0.42 mm × 2.4 mm for 16 channel prototype).
- Additional junction capacitance.
- Less expensive PCB technology.
- Much less demanding assembly techniques.
- No additional cost of SMD components.
- Specifically tuned for given type of MPGD.



Designed structures

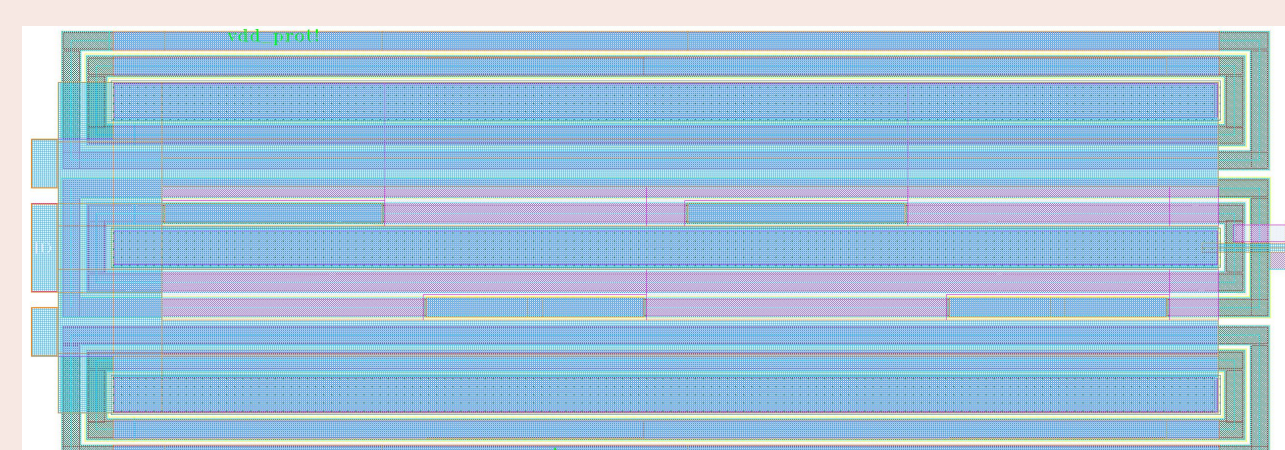
- Type A

Devices: one P- and one N-type diode.
Area: $2 \times 9500 \mu\text{m}^2$.



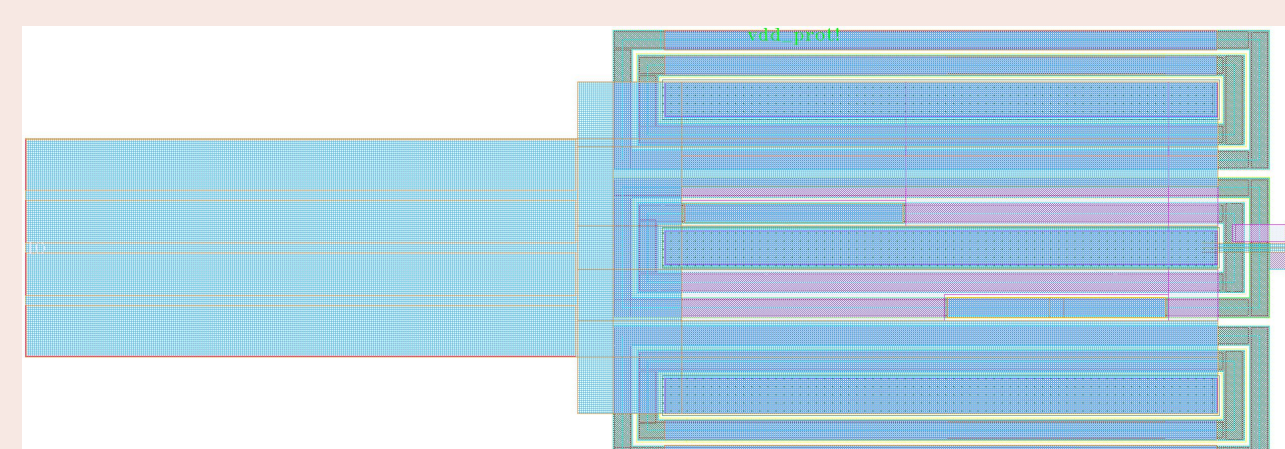
- Type B

Devices: one P- and two N-type diodes.
Area: $3 \times 5000 \mu\text{m}^2$.



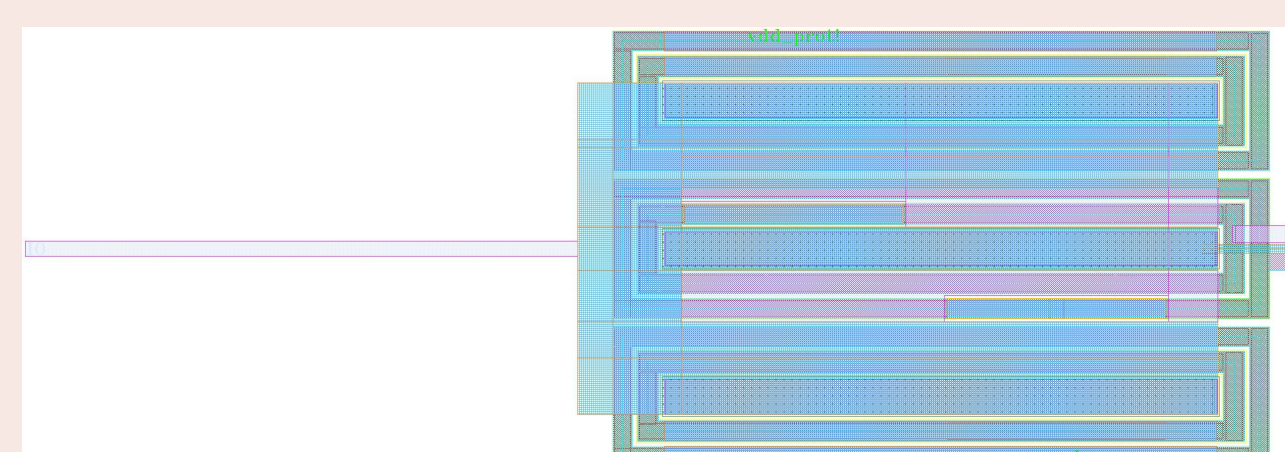
- Type C

Devices: one P- and two N-type diodes.
Area: $3 \times 2500 \mu\text{m}^2$.



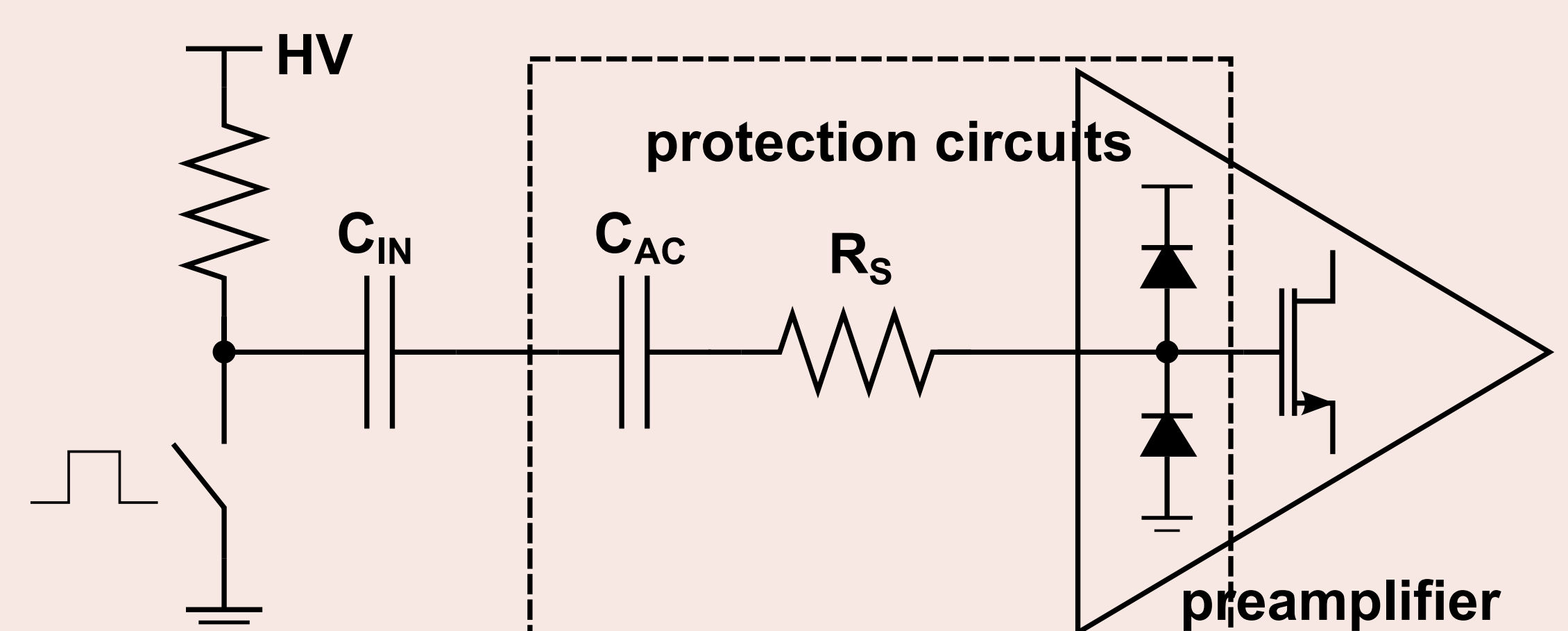
- Type D

Devices: one P- and two N-type diodes, additionally series 4Ω metal resistor.
Area: $3 \times 2500 \mu\text{m}^2$.



Discharge measurements

- Charge injected through 1nF capacitor C_{IN} .
- HV increased in 200 V steps from 0 to 1600 V.
- Standard tests: 5 pulses @ 0.5 Hz frequency.
- Aggressive tests: 10×100 pulses @ 0.5 Hz frequency.
- Different values of resistor R_S used (footprint 1206): 0, 10, 22, 68 Ω .
- For each HV level analogue performance of a given channel was measured.
- For structures A, B, and C no deterioration in the front-end performance was observed. Structures D worked properly only up to 250 V.



Acknowledgements

This work was supported by the National Science Centre (NCN) Poland, grant number DEC-2013/10/M/ST7/00568.