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Characterization of SLVS Driver and Receiver in a 65 nm CMOS Technology for High Energy Physics Applications

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This work presents the design and characterization of a SLVS transmitter/receiver pair, to be used for I/O links in High Energy Physics applications.

The prototype chip was designed and fabricated in the framework of the CHIPIX65 project and was completely characterized in the first quarter of 2016. The chip has been also irradiated with X-rays in order to evaluate the effect of the ionizing radiation on the signal integrity.

The full characterization of the driver and receiver will be discussed in the conference paper.

Summary

A transmitter/receiver pair designed for a possible integration in the RD53A prototype, and conform to the SLVS protocol, was designed in a 65 nm CMOS technology. The proposed link, that can be operated up to 1.2 Gbps, will be used in a harsh radiation environment, so the design is based on thin gate oxide transistors, using a supply voltage of 1.2 V. The SLVS standard describes a differential current-steering protocol with a voltage swing of ± 200 mV on a 100Ω termination resistance and a common mode of 200 mV. The driver architecture is based on a Bridged-Switch Current Source (BSCS) scheme. The 2 mA biasing current is switched through a 100Ω termination resistance, placed at the receiver input, according to the input data stream. The output current of the transmitter can be trimmed, by means of three configuration bits, in a range from 500 μ A to 2.5 mA. In order to achieve insensitivity to PVT variations, a simple low power common-mode feedback has also been included. The common mode voltage is sensed by two resistors, which are connected to the output nodes and compared with a reference voltage generated by a resistor voltage divider. The CMFB amplifier is based on a two stage Miller OTA. The receiver is based on three different stages: the first one is a fully differential amplifier with a cross-coupled load, rail-to-rail input stage, and with a bandwidth close to 1.2 GHz; the second stage is a differential-to-single ended amplifier with a full swing CMOS output voltage and the last one is a chain of three inverter. The receiver input is AC coupled for a possible use with serial powering. The common mode voltage of the signal at the input of the receiver is restored by resistor voltage divider. The chip was submitted in May 2015 and it was completely characterized during the first quarter of 2016. During the characterization activity, the input of the driver was stimulated with a CMOS Pseudo-Random-Bit Signal (PRBS). The signal integrity of the driver was evaluated by measuring the eye diagram at the termination resistance. The chip has also been irradiated, up to 550Mrad, with the X-rays machine present at CERN in order to evaluate the effect of the ionizing radiation on the signal integrity. The conference paper will report on the full experimental characterization of the SLVS transmitter and receiver.

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