A Low-Power and Low Transmission Latency Dual Channel Serializer ASIC for Detector Front-End Readout

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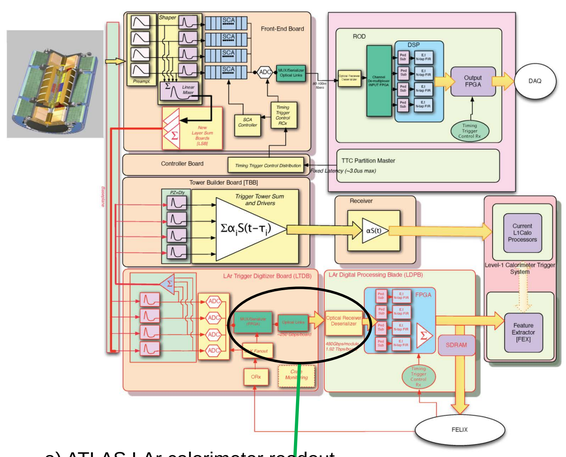
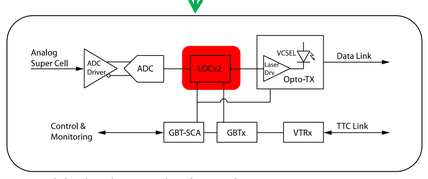
Introduction



a) ATLAS LAr calorimeter readout



b) LOCx2 chip in the optical readout system

LOCx2 and LOCx2-130 are High-speed serializer chips designed for the optical readout on the trigger digitizer board (LTDB) in the ATLAS Liquid Argon Calorimeter trigger upgrade project.

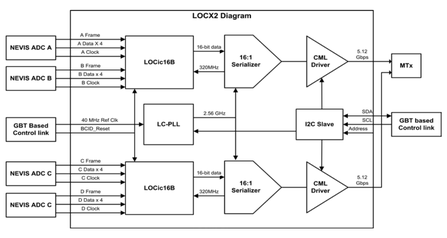
LOCx2 — the baseline design

- Based on a commercial 0.25 µm silicon-on-sapphire (SOS) CMOS technology
- Has two channels, each at 5.12 Gbps data, and consumes 950 mW.
- Each LOCx2 channel encodes data from two Nevis 4-channel-ADC chips or one 8-channel TI ADS5272 into the LOCic data frame
- Submitted LOCx2 in April 2016 and get chips back in September.
- The prototype chip has been preliminary test in lab and TID test.
- The final version chips are in production now.

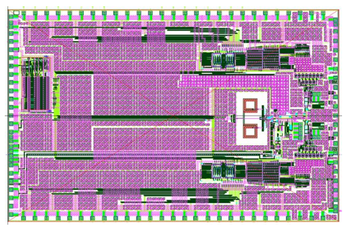
LOCx2-130 — a backup design of LOCx2

- A drop-in backup ASIC, pin compatible with LOCx2 except power supply voltage is 1.5 V.
- Using GF 0.13 µm bulk silicon CMOS process
- Two channels, each at 4.8 Gbps
- Reuse the analog PLL core from GBT, modified to be a shared PLL of two serializers.
- High-speed serializer core originally from GBT and modified version (TDS-SER chip) from University of Michigan.
- Implemented encoder and I2C slave in digital design flow
- Power consumption is 386 mW in estimation.
- Submitted LOCx2-130 in August, expect to get test chip in the end of 2016.

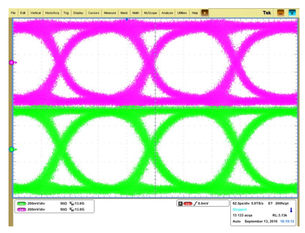
LOCx2 design and test



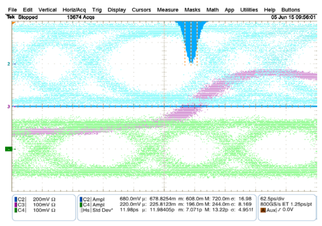
a) LOCx2 block diagram



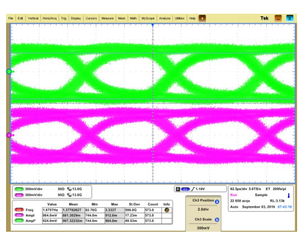
b) Die layout view



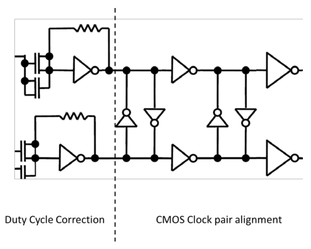
c) 2-channel eye-diagram, measured with chip soldered on board



d) Duty Cycle Distortion after radiation in prototype 2014



e) No DCD observed after TID test, measured with chip in socket

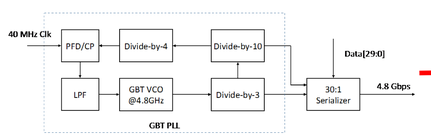


e) DCD correction and clock alignment circuits in current version

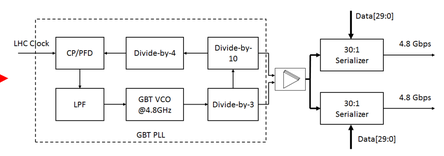
- Data transmission passes error check in FPGA board
- Add interface to TI ADS5272, works as expected
- Fixed the DCD issue after radiation in 2014 version.
- Programmable delay on-chip convenient for ADC interface

- Long-term reliability test is on-going
- SEE test is planned in this year.
- Production process is started
- QA test preparation is in-progress

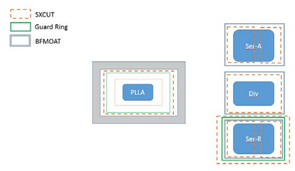
LOCx2-130 Design



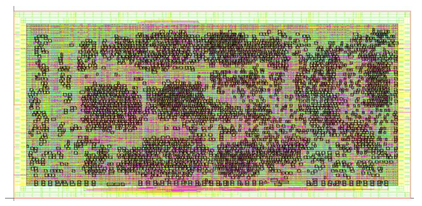
a) The diagram of TDS-SER core



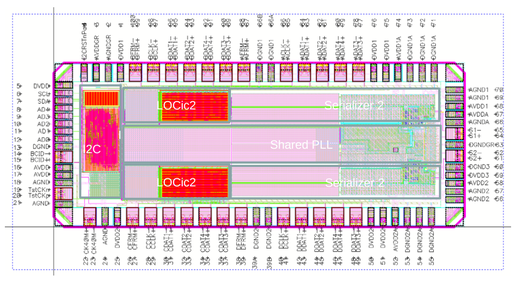
b) The diagram of LOCx2-130 core



c) Noise isolation scheme of PLL and serializers



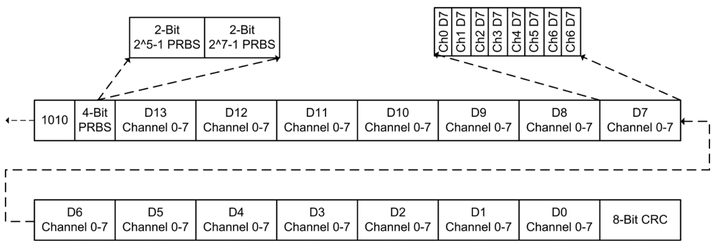
d) LOCic, data frame encoder, is implemented with digital design tool; layout view is shown



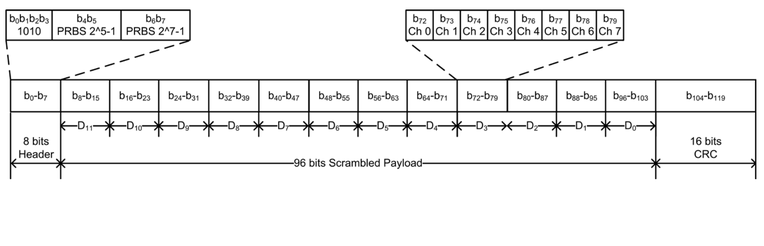
e) LOCx2-130 die layout

- Reuse proved GBT/TDS analog core
- Pin compatible design to LOCx2, reuse
- Same package is planned and confirmed
- Low power design with a shared PLL
- Noise isolation is carefully considered in design
- Edge-detection function is implemented to find optimal timing
- Full Triple module redundancy (TMR) design in digital circuits

Compare LOCx2 and LOCx2-130



a) 128-bit LOCic data frame



b) 120-bit LOCic data frame

LOCic data frame feature:

- Low overhead and latency, low re-synch time
- CRC8/CRC16 check data integrity in data transmission
- Transmitter 12-bit BCID information in header automatically

Why change to 120-bit LOCic data frame:

- Adapt to 4.8 Gbps data rate with GBT/TDS core
- Nevis ADC relaxed the data bits transmission from 14 bits per ADC channel to 12 bits.
- 128-bit data frame is reduced to 120-bit with similar structure in LOCx2-130
- LOCx2-130 also provides calibration mode to transmitter 14-bit ADC data without CRC protection

	LOCx2	LOCx2-130
Data rate	5.12 Gbps x 2	4.8 Gbps x 2
Latency(ns)	24.1-27.3	34.4-40.7
Encoder	128-bit LOCic frame	120-bit LOCic frame
Power consumption	950 mW (Measured)	386 mW (Estimation)
Slow control	I2C	I2C
ADCs supported	Nevis ADC, TI ADS5272/5294	Nevis ADC, TI ADS5272/5294
Die size	3860 um x 6036 um	2000 um x 5000 um
Package	QFN-100	QFN-100
Status	In production	Submitted

Acknowledgments

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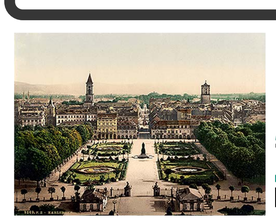
References

1. Hucheng Chen, Readout Electronics for the ATLAS LAr Calorimeter at HL-LHC, the Technology and Instrumentation in Particle Physics (TIPP) conference, Chicago, U.S.A, June 9-14, 2011.
2. H. Takai *et al.*, Characterization of COTS ADC radiation properties for ATLAS LAr calorimeter readout upgrade, TWEPP, Perugia Italy, September 23-27, 2013.
3. IEEE802.3 specification (2008), clause 49.



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