



Contribution ID: 124

Type: Poster

A Low-Power and Low Transmission Latency Dual Channel Serializer ASIC for Detector Front-End Readout

Wednesday, 28 September 2016 16:35 (1 minute)

We present design and test results of a dual-channel serializer ASIC, LOCx2, for detector front-end readout. LOCx2 interfaces an ASIC ADC, ADS5272 and ADS5294. LOCx2 may take data from any 12-bit or 14-bit, multiple channel ADCs with sampling rate from 32 to 43 MSPS. We also present the design of LOCx2-130, a drop-in backup to LOCx2 based a 0.13 μm bulk silicon CMOS process. Power consumption and transmission latency for LOCx2 is 900 mW (88 mW/Gbps) and 27 ns, and 350 mW (37 mW/Gbps) and 38 ns for LOCx2-130.

Summary

ASIC serializers are needed for particle physics detector front-end optical readout due to the demand on data bandwidth (about 200 Gbps per board), channel density, low power consumption, low transmission latency and radiation tolerance. LOCx2, an ASIC based a commercial 0.25 μm silicon-on-sapphire (SOS) CMOS technology, has been developed to meet the demands, in particular those from the optical readout on the trigger digitizer board (LTDB) in the ATLAS Liquid Argon Calorimeter trigger upgrade project. As we recently experienced prototype manufacturing difficulties in this SOS process, we developed a drop-in backup ASIC named LOCx2-130, using a 0.13 μm bulk silicon CMOS process. We submitted LOCx2 through an engineering run in April and plan to test in July and August, including irradiation tests. We plan to submit LOCx2-130 in August. We will present the design and test results of LOCx2, and the design of LOCx2-130.

LOCx2 has two serializing channels sharing one LC-VCO PLL. In each channel there is an interface block called LOCic that takes the upstream ADC data. LOCic is designed to interface ASIC ADCs, ADS5272 and ADS5294. With a programmable input timing adjustment, LOCx2 can take data from any 12-bit or 14-bit, 4 or 8 channel ADC chips that have a sampling rate from 32 to 43 MSPS and with serial outputs. LOCic prepares the data for serial transmission using a custom encoder. An 8-bit CRC in each transmission frame is used to detect possible bit flip errors. The serializer in LOCx2 is 16:1 followed by a CML output driver, working at 5.12 Gbps. LOCx2 is configured and controlled through I2C. According to the post layout simulations, LOCx2 consumes 900 mW under a 2.5 V power supply when both channels function at the design speed of 5.12 Gbps. The transmission latency is 27 ns. A previous prototype measures 850 mW and 27 ns for power consumption and latency, respectively.

LOCx2-130 has a similar interface to that in LOCx2. This interface is digitally synthesized with the transmission latency minimized. LOCx2-130 can transmit 16 channels of ADCs, with 12-bit or 14-bit in each channel. In the case of 12-bit, a 16-bit CRC is used for error detection. There is no error detection when 14-bit ADCs are connected. The serializer and the PLL are adapted from a design that originates from the GBTx ASIC. The I2C here and the one in LOCx2 are adapted from CERN's IP. According to the post layout simulations, LOCx2-130 consumes 350 mW under a 1.5 V power supply when both channels function at the design speed of 4.8 Gbps. The transmission latency is no more than 38 ns.

Both LOCx2 and LOCx2-130 will be packaged in plastic QFN100. The tests will be carried out using a clamp socket. Testing results and knowledge obtained on QFN packaging and testing with clamp socket will be reported.

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Session Classification: POSTER

Track Classification: ASIC