Development of 32-Channel System for Processing Asynchronous Data from the CBM GEM Detectors

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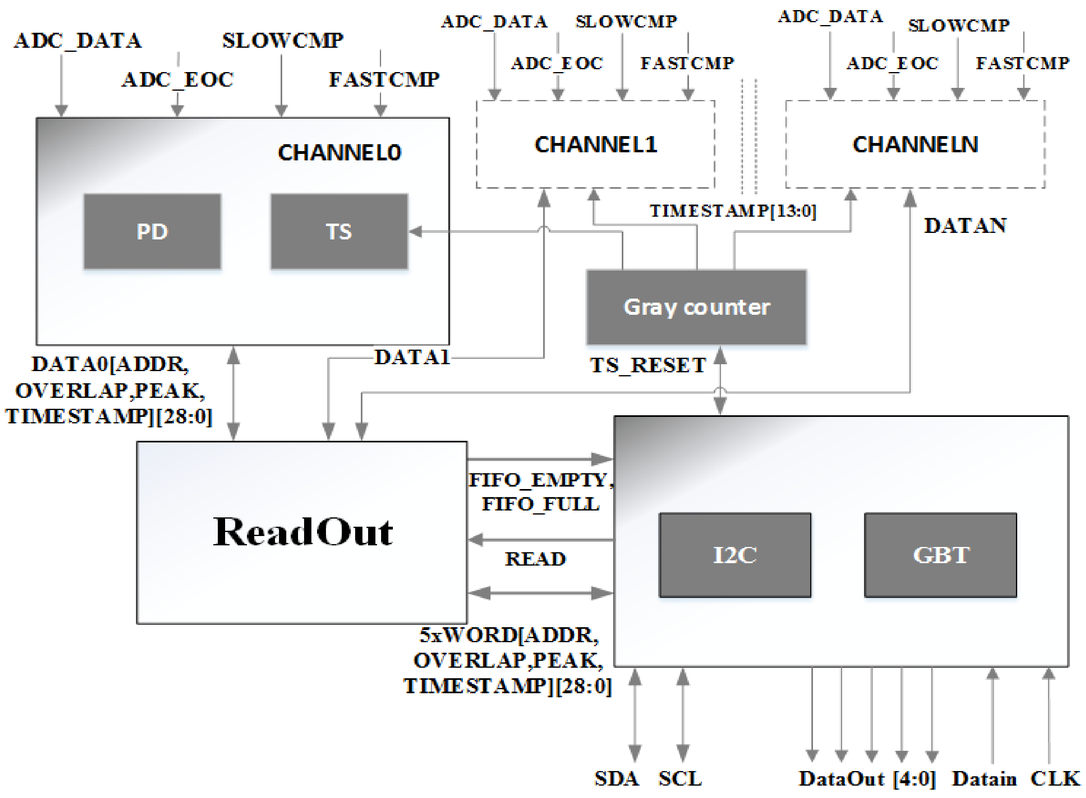
The paper describes the elaboration of the 32-channel system of processing the asynchronous data from the CBM muon chambers at FAIR. GEM detectors are supposed to be used to restore muon tracks, appearing as result of accelerator beam interaction with a fixed target. The readout electronics should be asynchronous. The total number of channels exceeds 10^6, while the minimal inter-event time is 100 ns. For each channel the ASIC should provide the measurements of signal amplitude, its arrival time and channel number, keeping power consumption within 10 mW/channel.

The system provides the generation of data packages, consisting of the digital codes of signal amplitude, timestamp (TS) and channel number. Control and data exchange with host are provided by 2 serial interfaces: the slow I2C one and the high-speed GBT (320 MHz) one.



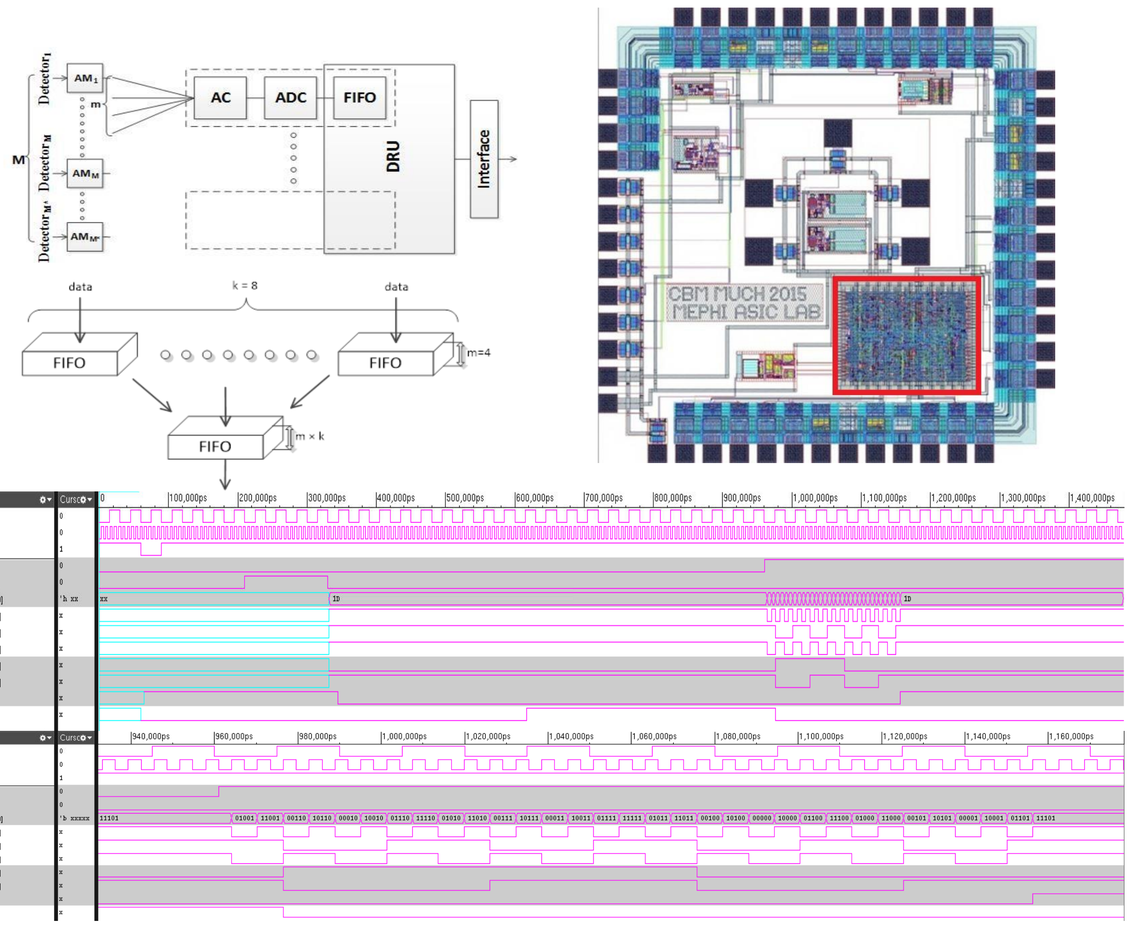
Picture 1 Schematic diagram from 32-channel ICs.

The first 8-channel prototype is intended for debugging the functional model. It's digital block performs the following functions:

- load of initial data and control commands;
- picking up the information about input signals ;
- high-speed (320 MHz) serialization of output data;
- test signals are applied to the system by built-in ADC emulators;

The ASIC has the following main characteristics:

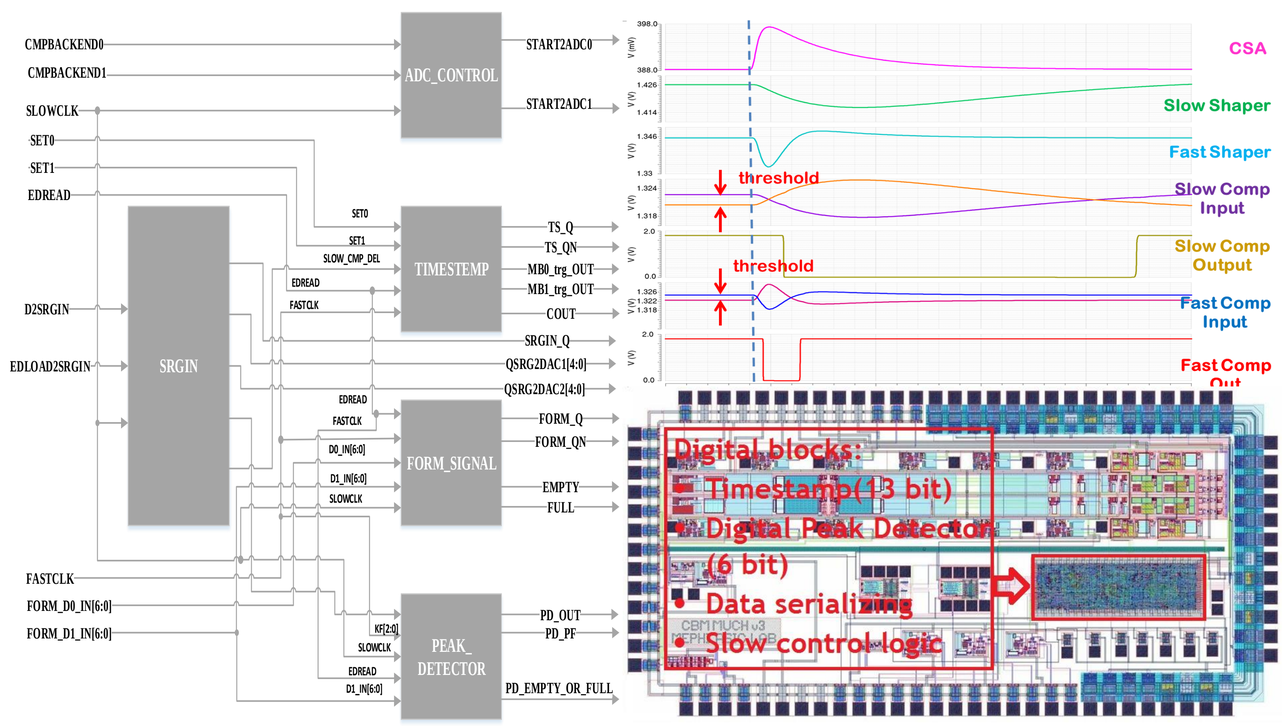
- ADC emulators - maximal speed for 5-bit data - 50 MHz;
- Readout block: 32 FIFO (22 bit, addr=4) Fwrite - 320 MHz, Fread – 50 MHz, Power consumption is 43 mW and digital block area is 450x450 μm^2;



Picture 2 First prototype ASIC, digital part scheme diagram and simulation.

The digital part in the second chip prototype calculates the digital codes pf timestamp and signal amplitude.

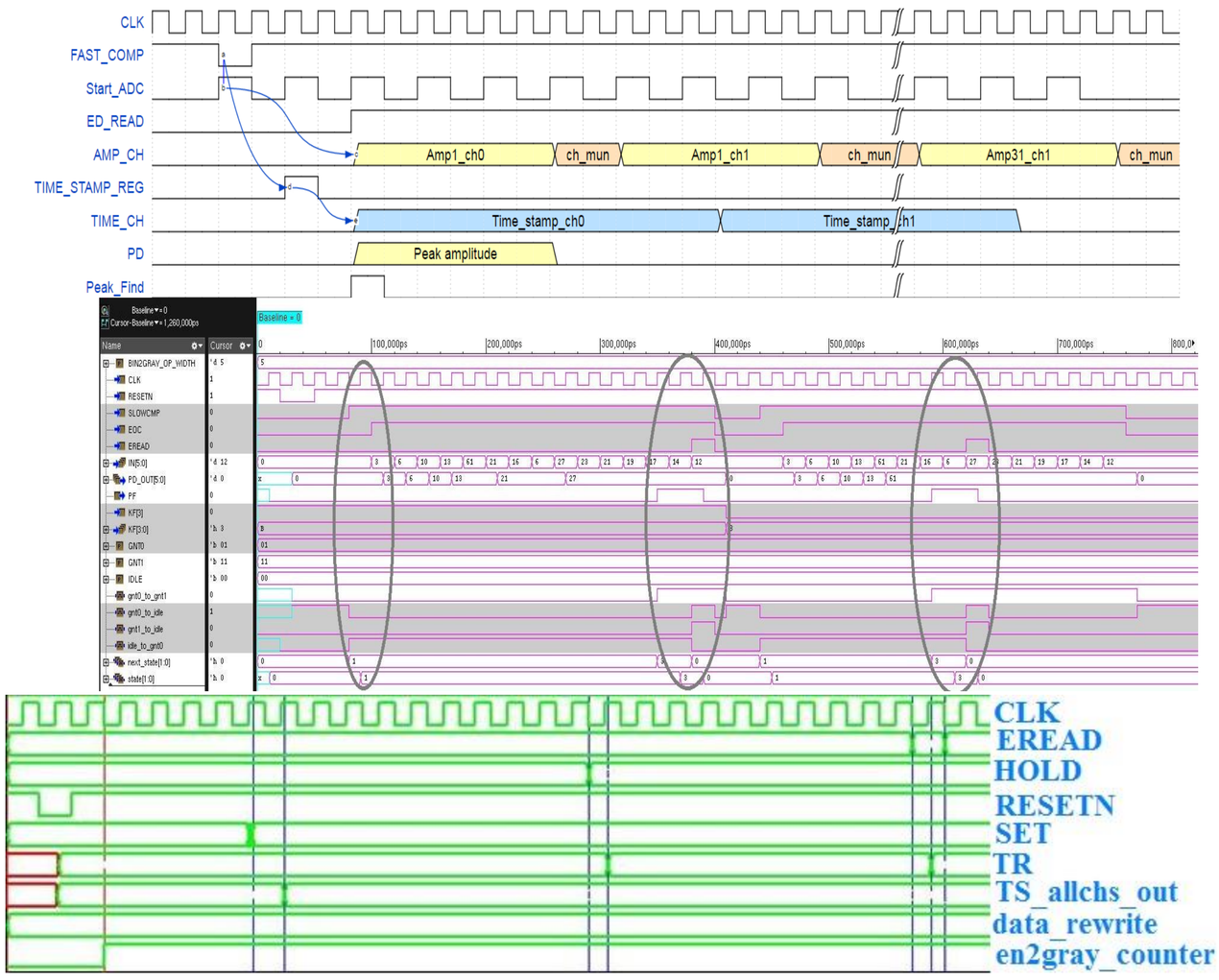
Analog channels (processing GEM detectors signals) consist of:
CSA (signal amplification), slow SH (amplitude), fast SH (TS), comparators (signal sign) and 6-bit ADC(digitalizing signals).



Picture 3 Analog Channel in second prototype ASIC, schematics and simulation.

Timestamp block (TS) consists of 2 parts: multi-channel part and the one of a common 29-bit gray counter for all channels. Timestamp code is stored in a channel register when the fast comparator signal switches from low to high logical level. During time T the TS block waits for slow comparator signal to have a high logical level approving the validity of the stored TS code. F = 320 MHz, Power consumption is 6 mW(3mW/channel) and digital block area is 120x120 μm^2.

Peak detectors block – calculates the average of 3 comparator switching's and compares it with the input signal multiplied by the correction factor. If the average is greatest, the signal is assumed as a true one, and a record to the shift register is done. Then the search of peak is accomplished. Otherwise the signal is regarded false. F = 50 MHz, Power consumption is 180 uW and digital block area is 105x105 μm^2.



Picture 4 Second prototype ASIC, peak detector, timestamp simulation.

Conclusion

The results of design and laboratory tests of the prototype chip as well as the development of the backend part have proved the relevance of the presented 32-channel system design. The next step is expected to be the manufacture and tests of the full-scaled 32-channel version.

Acknowledgement

This work was supported by Grant No. 14.A12.31.0002, issued by the Russian Federation Ministry of Education and Science according to the RF Governmental resolution No 220.

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