Contribution ID: **134** Type: **Poster**

Development of 32-Channel System for Processing Asynchronous Data from the CBM GEM Detectors

Tuesday 27 September 2016 16:45 (1 minute)

The 32-channel system for processing asynchronous data from the GEM detectors is presented. It has been developed as part of ASIC intended for the muon chamber of the CBM experiment and allows to run up to 10 MHz channel rate.
The system provides the generation of data packages, consisting of the digital codes of signal amplitude, arrival time and channel number. Control and data exchange with host are provided by 2 serial interfaces: the slow I2C one and the high-speed (320 MHz) one.
The results of testing the main blocks, prototyped in UMC CMOS 180nm process are given.

Summary

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The paper describes the elaboration at the 32-channel system of processing the asynchronous data from the CBM muon chambers at the FAIR. GEM detectors are supposed to be used to restore muon tracks, appearing as result of accelerator beam interaction with a fixed target. The readout electronics should be asynchronous. The total number of channels exceeds 106, while the minimal inter-event time is 100 ns. For each channel the ASIC should provide the measurements of signal amplitude, its arrival time and channel number, keeping power consumption within 10 mW/channel.
An 8-channel prototype of system was elaborated for debugging the functional model. It comprises the blocks, performing the following functions: load of initial data and control commands, picking up the information about input signals as well as the high-speed (320 MHz) serialization output data. Test actions are applied to the system by built-in ADC emulators.
The prototype has a pyramidal structure, consisting of several FIFO blocks and a control one. It was manufactured via Europractice in the UMC CMOS 180 nm process. Designed for lab tests board includes the input/output analog and digital interfaces for data exchange with FPGA processing board.
The tests showed the following characteristics: maximal speed for 5-bit data - 50 MHz, readout one from the output FIFO - 320 MHz. Power consumption and chip area are 43 mW and 450x450 μm sq correspondingly. As result of testing one may conclude that in full scaled version it is expedient to use the single-level pyramidal structure of data acquisition based on FIFO.
The timestamp block was optimized for the 32-channel system. Despite of an enhanced immunity to failures, the use of majoritarian logic with tripling, realized in the prototype chip, is considered to be non-optimal in terms of chip area. Thus the block structure has been simplified to a common time counter in the Grey code for all channels, control logic, using a non-majoritarian principle of enhancing reliability, and timestamp registers in each channel.
The system features an early stage signal digitization. For amplitude measurements there was designed a digital peak detector block. The function of correcting false operation and noise filtration is built-in the block.
The interface block accomplishes a multilevel synchronisation with the GBTX chip, according to its exchange protocol. Synchronization errors are checked by CRC codes and control commands. The reference frequency is set by an external clock of 160 MHz. The control of the ASIC parameters and output data transmission is carried out at a speed up to 320 MHz.

Thus the results of laboratory tests of the prototype chip as well as development of the backend part has proved the relevance of the presented system design. The next step is expected to be manufacture and test the full-scaled 32-channel version.

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Session Classification: POSTER

Track Classification: ASIC