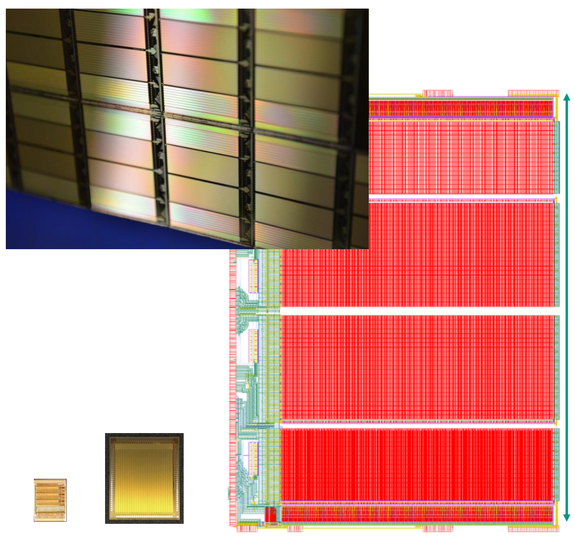
HVCMOS Sensors for the High Luminosity Upgrade of ATLAS Experiment: The Second Generation of Prototypes and their Electronic Blocks

Roberto Blanco[1]

Hui Zhang[1], Ivan Peric[1], Christian Krämer[1], Richard, Leys[1], Mridula Prathapan[1], Alena Weber[1], Felix Ehrler[1], Rudolf Schimassek[1]

Institute for Data Processing and Electronics

[1]KIT-ADL (ASIC and Detector Laboratory)

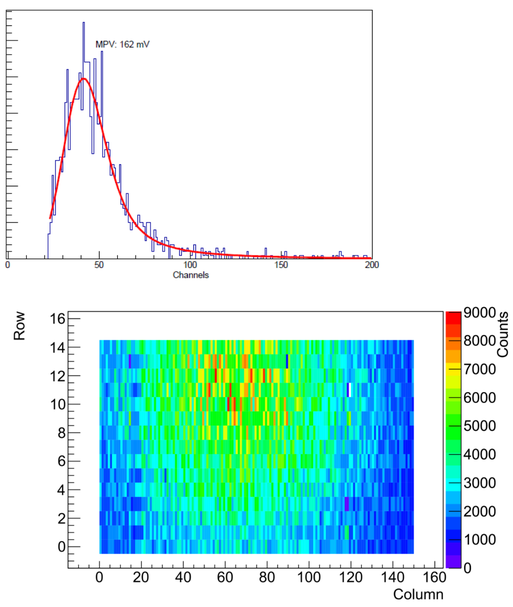


Tested: excellent efficiency and time resolution after irradiation

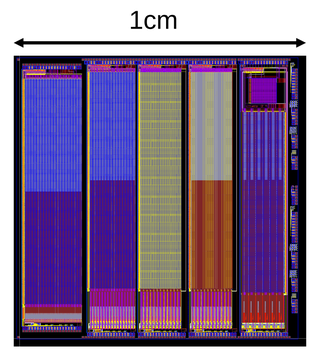
1st generation

Produced, tests started recently

2nd generation



Tests at KIT, monolithic readout



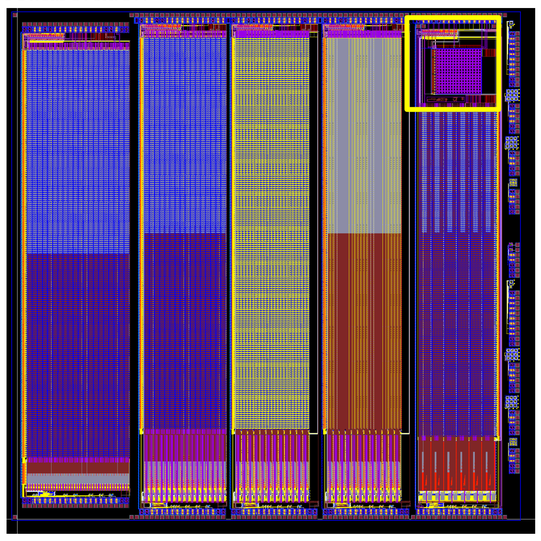
LF-HVMAPS

Submitted

Mu3e (also for ATLAS) Analog pixels Untriggered readout	ATLAS Digital pixels (with comparator) Triggered readout	ATLAS Digital pixels Untriggered readout	Test structures

Submitted in August 2016

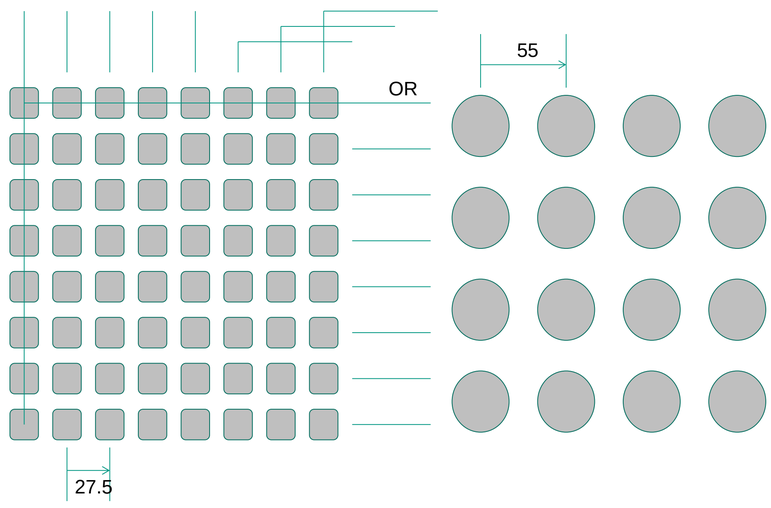
This August (2016) we have submitted 6 matrices as five chips in **LFA15 process** (150nm) on different high resistive substrates. The total reticle size is 1 x 1 cm
Similar designs will be realized in **H18 technology** and submitted beginning of October.
The project has been performed within HVCMOS collaboration



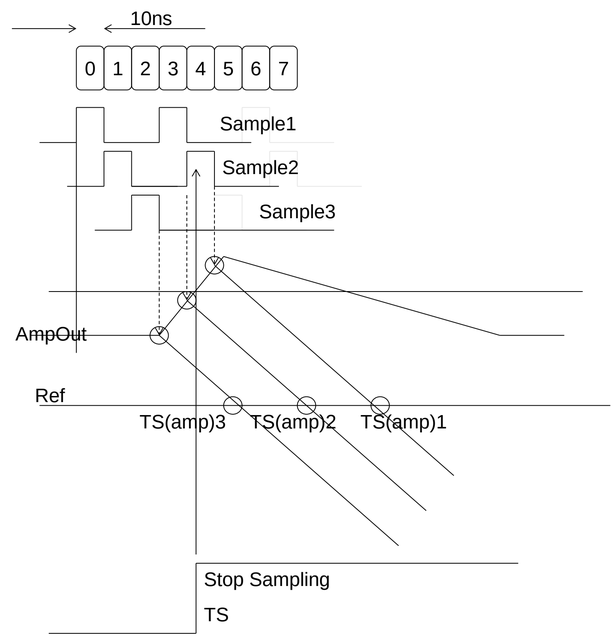
The five matrices are the full featured monolithic matrices. They can be distinguished by the readout cell type, the pixel type and the pixel address multiplexing.

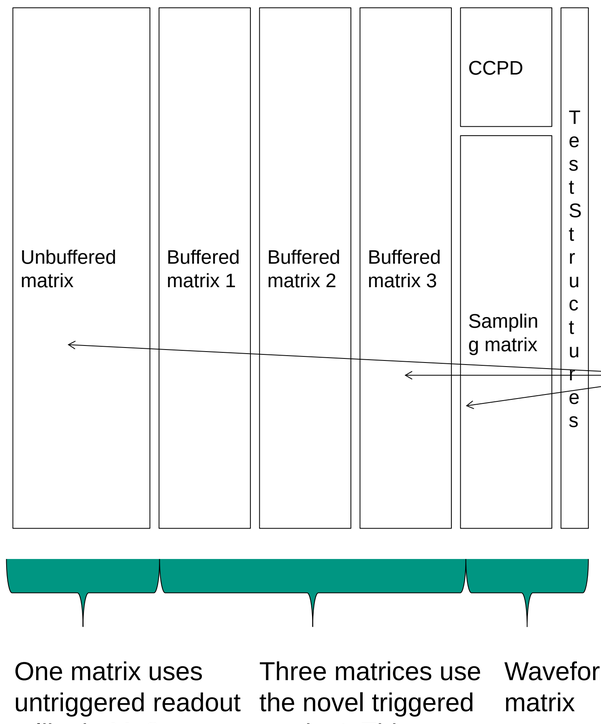
The pixel contains CSA, comparator, edge detector, pulse stretcher and threshold tune circuit.

Capacitive coupled pixel detector (CCPD):
One matrix is a CCPD with small pixels (27.5um x 27.5um) that can be readout by the TimePix chip. (Next version for RD53 ROC is planned)



Waveform sampling:
One matrix uses the readout (untriggered) with the waveform sampling capability. The analog waveform is sampled with 8 – bit resolution, 6 times around the threshold crossing point. It can be 6 samples before the threshold crossing or 3 times before and 3 times after. The sampled voltages are immediately digitized (by 6 simple ADCs) and the digital values stored. Every pixel has its sampling blocks – we have 6 ADCs per pixel. The pixel size is 40 x 250um. With this novel sampling capability we would like increase the time resolution of HVCMOS sensors.

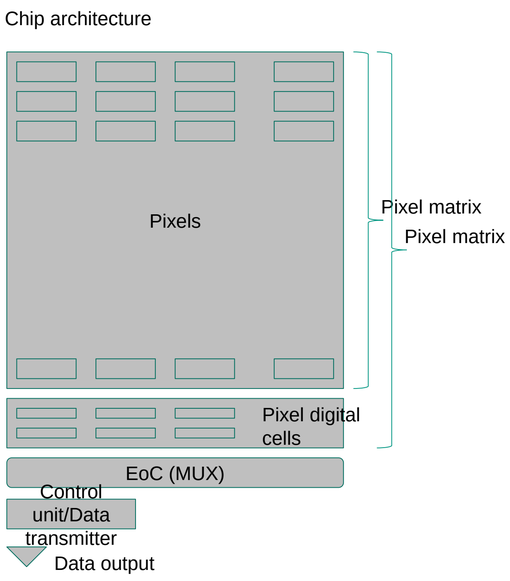




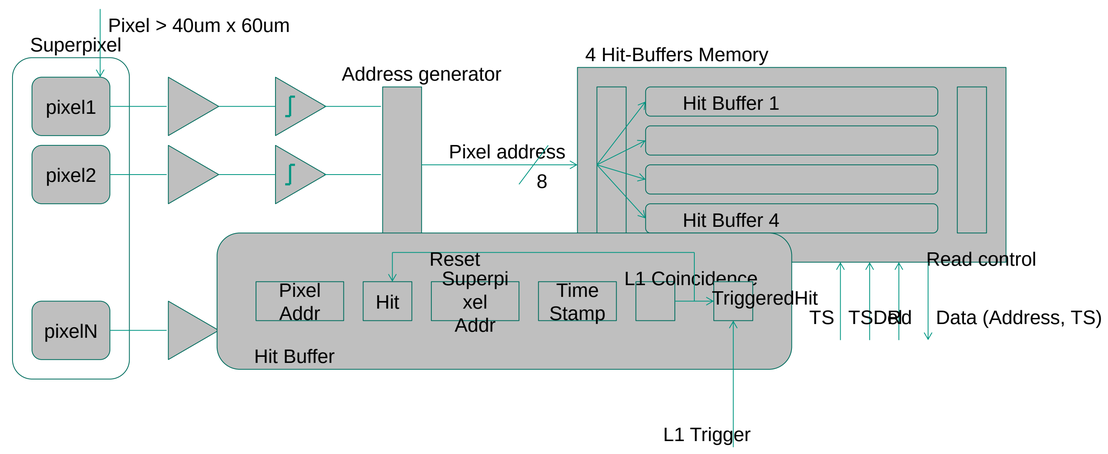
One matrix uses untriggered readout – like in Mu3e or H35DEMO (based on FEI3) circuit.

Three matrices use the novel triggered readout. This readout allows trigger delay of up to 25us.

Waveform sampling matrix



Triggered readout:
A group of 8 or 16 pixels is attached to a readout trigger buffer block. The block has 4 cells that are identical. The hit OR stores the 8 local address bits into the first empty trigger buffer. After the trigger delay the buffer is either emptied (if no trigger) or marked for readout (if trigger is present). This scheme can cope with rather high occupancy. Number of buffer cells may be adjusted later. The size of the block (4 buffers) is only 40um x 100um.



Institute for Data Processing and Electronics

Contact:
M.Sc. Roberto Blanco
Email: roberto.blanco@kit.edu
Phone: +49 721 608-28697