HVCMOS Sensors for the High Luminosity Upgrade of ATLAS Experiment: The Second Generation of Prototypes and their Electronic Blocks

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This August [2016] we have submitted 6 matrices as five chips in LFA15 process (150um) on different high resistive substrates. The total reticle size is 1 x 1 cm. Similar designs will be realized in M18 technology and submitted beginning of October. The project has been performed within HVCMOS collaboration.

The five matrices are the full featured monolithic matrices. They can be distinguished by the readout cell type, the pixel type and the pixel address multiplexing. The pixel contains CSA, comparator, edge detector, pulse stretcher and threshold tune circuit.

Waveform sampling:
One matrix uses the readout (untriggered) with the waveform sampling capability. The analog waveform is sampled with 8—bit resolution, 6 times around the threshold crossing point. It can be 6 samples before the threshold crossing or 3 times before and 3 times after. The sampled voltages are immediately digitalized (by 6 simple ADCs) and the digital values stored. Every pixel has its sampling blocks — we have 6 ADCs per pixel. The pixel size is 40 x 250um. With this novel sampling capability we would like increase the time resolution of HVCMOS sensors.

Triggered readout:
A group of 8 or 16 pixels is attached to a readout trigger buffer block. The block has 4 cells that are identical. The hit OR stores the 8 local address bits into the first empty trigger buffer. After the trigger delay the buffer is either emptied (if no trigger) or marked for readout (if trigger is present). This scheme can cope with rather high occupancy. Number of buffer cells may be adjusted later. The size of the block (4 buffers) is only 40um x 100um.

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