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HVCMOS Sensors for the High Luminosity Upgrade of ATLAS Experiment: The Second Generation of Prototypes and their Electronic Blocks

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HVCMOS sensors and capacitive coupled pixel detectors (CCPD) are seen as an option to the standard sensor technologies such as hybrid- or strip-detectors for several particle physics experiments, among others ATLAS. The latest important achievement of this development is the production of first reticle size HVCMOS sensor –H35DEMO - that can be readout either as a monolithic detector, with the readout electronics on the chip, or attached to an external readout chip in form of a CCPD. H35DEMO is currently being tested and the first results are very good.

Summary

Our group is working on the development of HVCMOS sensors and capacitive coupled pixel detectors (CCPD) since 2006. These sensors are seen as an option to the standard sensor technologies such as hybrid- or strip-detectors for several particle physics experiments, among others ATLAS. The latest important achievement of this development is the production of first reticle size HVCMOS sensor –H35DEMO - that can be readout either as a monolithic detector, with the readout electronics on the chip, or attached to an external readout chip in form of a CCPD. H35DEMO is currently being tested and the first results are very good.

In parallel with the demonstration that a HVCMOS sensor fulfils the ATLAS specifications, we are working on several more advanced large area prototypes with nearly complete electronics, i.e. with the system architecture that could be used in the experiment. The submission of the corresponding designs is planned for July 2016. Some of the possible scenarios for the application of HVCMOS sensors in ATLAS are: The use of monolithic sensors in the outer pixel layers. The use of capacitively- or DC-coupled pixel detectors based on a HVCMOS sensor and a new readout chip in the inner pixel layer. The goal is a pixel seize of 25um x 25um or less. The use of HVCMOS segmented-strip sensors in the outer tracker regions. Finally, we are considering HVCMOS layers that could generate track trigger. For all of these application cases, dedicated electronic blocks have been developed in our group. For the monolithic sensors we have developed very small, content addressable memory cells that can be used to keep the particle-hit information for relatively long time > 25us and to detect the coincidence of the hit information with a trigger signal. For instance a cell designed in a 180nm process occupies an area of only about 8um x 80um and can store the information coming from four pixels. For the CCPD-sensors designed for the inner pixel layers, we have developed small HVCMOS pixels and the small readout blocks that can be used in the new readout chip. For the track trigger layers, we are designing high-rate and low-latency particle hit data readout blocks. This contribution will give the overview of different readout architectures and the design details of the most important building blocks.

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