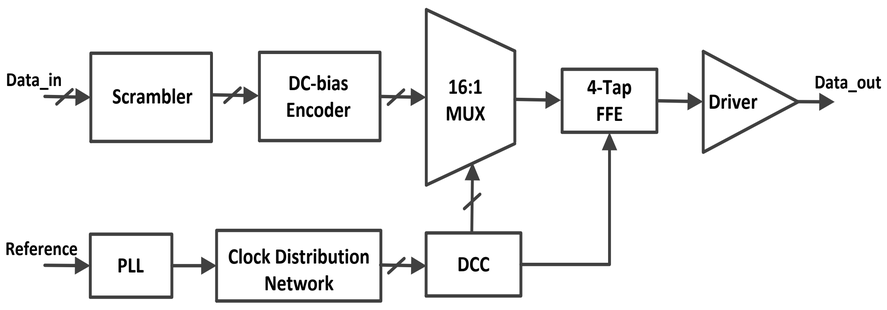
A Low-Power 10 Gbps Serial Link Transmitter ASIC for Particle Detectors in 65nm CMOS

Yulang Feng[a], Jinghong Chen[a], Qinjun Fan[a], Yuxuan Tang[a], Zhiheng Zuo[a], Datao Gong[b], Tiankuan Liu[b], and Jingbo Ye[b]
[a] *Department of Electrical and Computer Engineering, University of Houston, Houston, TX 77004, USA*
[b] *Department of Physics, Southern Methodist University, Dallas, TX 75275, USA*
yfeng19@uh.edu, jinghong@uh.edu

Introduction

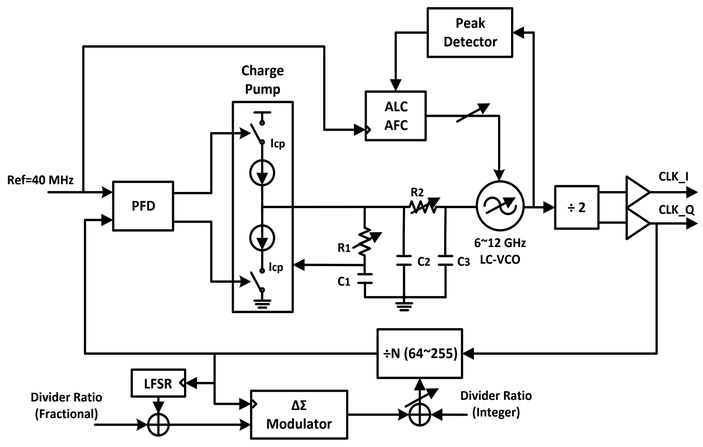
- High-speed low-power and radiation-tolerant data links are critical for the large volume data transmission in particle detection experiments
- A 10 Gbps low-power serial link transmitter is developed in a 65nm CMOS technology
- This serial link transmitter mainly includes a low-jitter Σ-Δ fractional-N PLL for clock generation, a power-efficient 16:1 serializer and a CML driver
- The PLL has been designed and tested and achieved a 6-to-12 GHz frequency tuning range and a RMS jitter of 0.67 ps
- This serializer with on-chip PLL is being submitted for fabrication and simulation results indicate a power efficiency of 9.8 mW/Gbps at 10 Gbps data rate

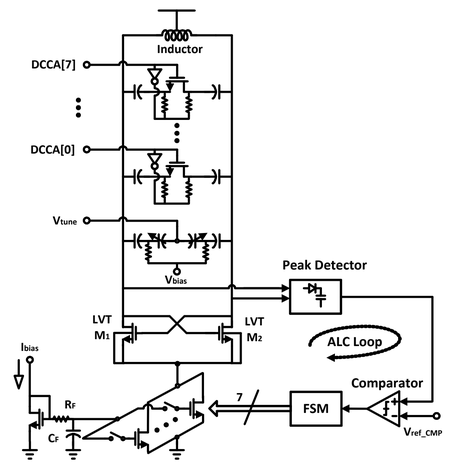
Architecture



- The transmitter consists of a scrambler, a DC-bias encoder, a 16:1 mux and a 4-Tap FFE followed by a programmable output driver
- An LC VCO fractional-N PLL provides the clock signal to the serializer
- Since half-rate serialization is prone to DCD, a DCC (duty cycle corrector) is designed achieving a tight timing control and accuracy

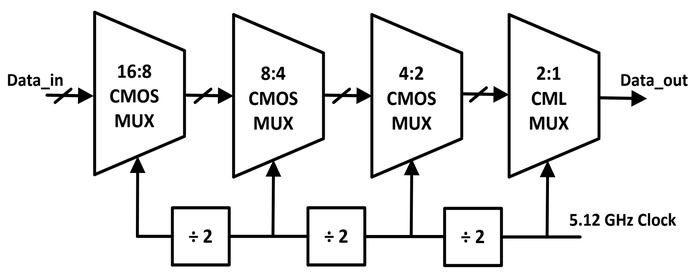
Wideband and Low-jitter PLL

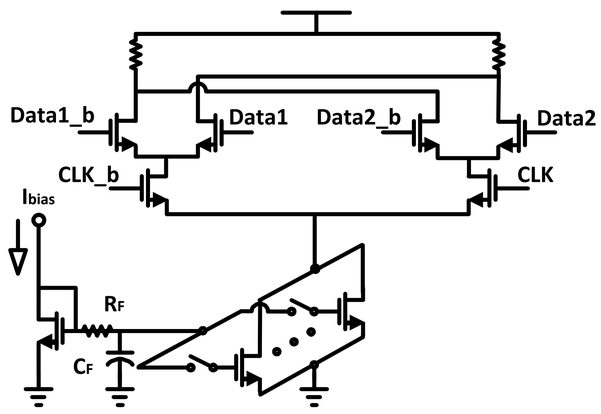




- The PLL is designed to cover an octave frequency from 6 GHz to 12 GHz
- The loop bandwidth is optimized to tradeoff the in-band and out-band noises
- The VCO core consists of a single-turn inductor, an 8-bit binary weighted digitally-controlled MIM capacitor array (DCCA), accumulation-mode varactors, and a digitally-controlled automatic leveling control loop

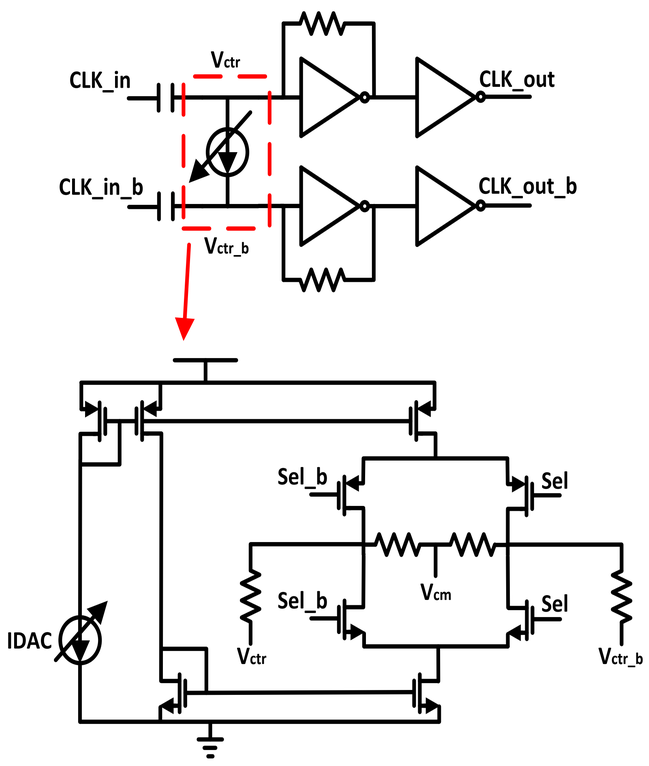
Power-Efficient 16:1 Serializer





- To improve power efficiency, the first 3 stage 2:1 muxes are implemented using CMOS logic gates while the last 2:1 mux is based on CML logic gates
- The low-speed stages are protected by TMR and the high-speed stages are designed with SEE immunity on the sensitive nodes
- To adjust the output swing, the tail current of the CML driver is designed to be programmable

Programmable DCC

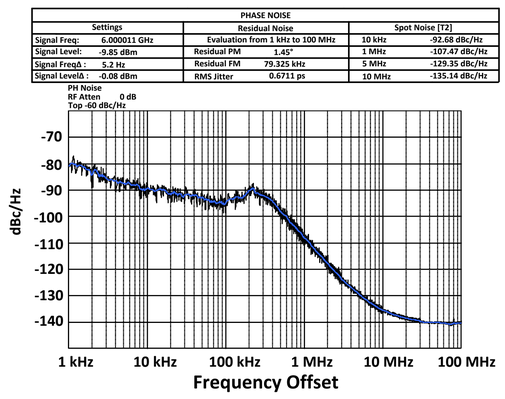


- To mitigate the duty cycle distortion, a programmable DCC is implemented by adding a small DC voltage at the inverter input node
- The DC voltage is adjusted by switched-programmable current (IDAC)

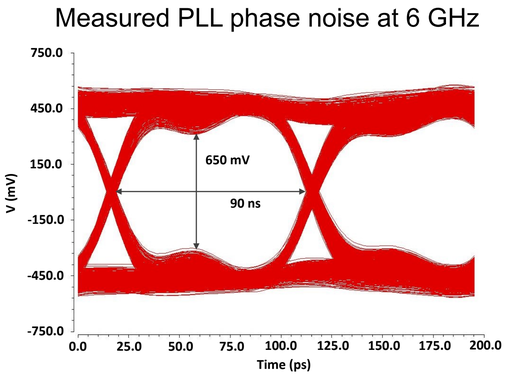
SERIAL DATA LINK PERFORMANCE

Technology	65nm CMOS
Data Rate	10 Gbps
PLL Random Jitter (RMS)	0.67 ps
Power Consumption	98 mW
TX EQ	4-Tap FFE
Power Efficiency	9.8 mW/Gbps

- 65nm CMOS
- Data rate of 10 Gbps
- Supply voltage of 1.2 V
- TX swing 200~800 mVppd
- Power consumption of 98 mW



Measured PLL phase noise at 6 GHz



Simulated eye-diagram of the "Serailzier + PLL" ASIC at 10 Gbps

PERFORMANCE COMPARSION

Ref	Process	VDD	TX EQ	TX Power Efficiency	TX RJ (rms)	TX Swing
[1]	45nm SOI	1.2 V	DPWM	6.2 mW/Gbps @10 Gbps (w/ PLL)	1.3 ps	N/A
[2]	90nm CMOS	0.8 ~ 1.2 V	2-Tap FIR	1.26 mW/Gbps @6 Gbps (w/o PLL)	N/A	100 ~ 400 mVppd
[3]	90nm CMOS	1.2 V	Current Mode	0.6 mW/Gbps @3.2 Gbps (w/ PLL)	4.6 ps	100 mVppd
[4]	130nm CMOS	1.2 V	N/A	1.3 mW/Gbps @10 Gbps (w/o PLL)	N/A	1.2 Vppd (PAM-4)
This Work	65nm CMOS	1.2 V	4-Tap FFE	9.8 mW/Gbps @10 Gbps (w/ PLL)	0.67 ps	200 ~ 800 mVppd

Conclusion

- A 10 Gbps serial data link with a built-in and low-jitter PLL is designed in a 65nm CMOS technology
- The LC-VCO PLL is tested and achieved a frequency tuning range from 6 GHz to 12 GHz with an RMS jitter of 0.67 ps
- The serial data link is submitted for fabrication and simulation results show a power efficiency of 9.8mW/Gbps at 10 Gbps data rate

References

[1] W. Wang et al, "A 10-Gb/s, 107mW Double-Edge Pulse-width Modulation Transceiver," IEEE Trans. Circuit Syst. I, April 2014.
[2] Y.-H. Song et al, A 6-Gbit/s hybrid voltage-mode transmitter with current-mode equalization in 90-nm CMOS, IEEE Trans. Circuits Syst. II, Aug. 2012.
[3] Rajesh Inti et al., "A Highly Digital 0.5-to-4Gb/s 1.9mW/Gb/s Serial Link Transceiver Using Current-Recycling in 90nm CMOS," in IEEE ISSCC'2011.
[4] B. Song et al, A 13.5-mW 10-Gb/s 4-PAM serial link transmitter in 0.13-μm CMOS technology, IEEE Trans. Circuits System II, Express Briefs, 2014.

TWEPP 2016 - Topical Workshop on Electronics for Particle Physics,
September 26 - 30, 2016, Karlsruhe Institute of Technology, Karlsruhe, Germany