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A Low-Power 10 Gbps Serial Link Transmitter ASIC for Particle Detectors in 65nm CMOS

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This paper presents a 10 Gbps serial link transmitter ASIC designed in a 65 nm CMOS technology. The ASIC mainly includes an LC-VCO PLL, a 16:1 serializer and a CML driver. Simulation results show that the PLL achieves a 6-to-12 GHz tuning range and an RMS jitter of 0.67pS. The serializer has a deterministic jitter of 11 pS and a programmable output swing from 200mV to 800mV (pk-pk). The PLL and the serializer consumes 53.6 mW and 73mW from a 1.2V power supply, respectively.

Summary

The large volume data production in recent high energy physics experiments requires high speed data links between the on-detector and off-detector subsystems. This paper presents a low-power 10 Gbps serial link ASIC in a 65nm CMOS technology. The ASIC includes a low-jitter LC-VCO PLL, a data scrambler and DC-balance encoder, a 16:1 serializer and a CML output driver.

A charge-pump Σ-Δ fractional-N PLL is developed for clock generation. The major challenge for the PLL is to achieve low jitter and SEE robustness. An LC oscillator is chosen because of its low noise performance. The PLL works in either integer-N or fractional-N mode. Programmable resistors in the loop filter along with programmable charge pump current provide control over loop bandwidth against different VCO gains and divider ratios. The PLL loop bandwidth is optimized to tradeoff the in-band and out-band noises. The PLL is designed to cover an octave frequency from 6GHz to 12GHz. NMOS negative transconductance is adopted due to its lower parasitic. The inductors of the VCO is optimized for high Q-factor as well as wide tuning range. The VCO core consists of a single-turn inductor, an 8-bit binary weighted digitally-controlled MIM capacitor array (DCCA), accumulation-mode varactors, and a digitally-controlled automatic leveling control loop. Since the required negative transconductance varies with the oscillation frequency, the biasing current is made programmable to ensure the oscillator to operate at the edge of the current-limited regime for a maximum voltage swing without excessive waste of power. The clock distribution network consists of buffers, divider-by-2 and multiplexers to deliver the final clock signals.

The high-speed serializer is a 16:1 multiplexer with a 4-stage binary-tree structure, namely 16:8, 8:4, 4:2 and 2:1 multiplexer in a chain. The 4 multiplexer stages are driven by 0.64, 1.28, 2.56 and 5.12 GHz clock signals, respectively. The low-speed stages are protected by TMR and the high-speed stages are designed with SEE immunity on the sensitive nodes. The serializer provides a complementary signal to a CML driver, which drives a 50 Ω impedance trace to the VCSEL driver in an optical module.

The 10 Gbps serial link transmitter ASIC is designed in a 65-nm CMOS process. Simulation results indicates the PLL achieves a 6-to-12 GHz tuning range and an RMS jitter of 0.67pS. The serializer has a deterministic jitter of 11 pS (pk-pk) and its output swing can be programmed from 200mV to 800mV (pk-pk). The power consumption of the PLL and the serializer including the CML driver are 53.6 mW and 73mW from a 1.2V power supply, respectively. The 10 Gbps serial link ASIC will be submitted for fabrication in August. Extensive electrical and radiation performance testing will be carried out and the testing results will be provided in the final paper.

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