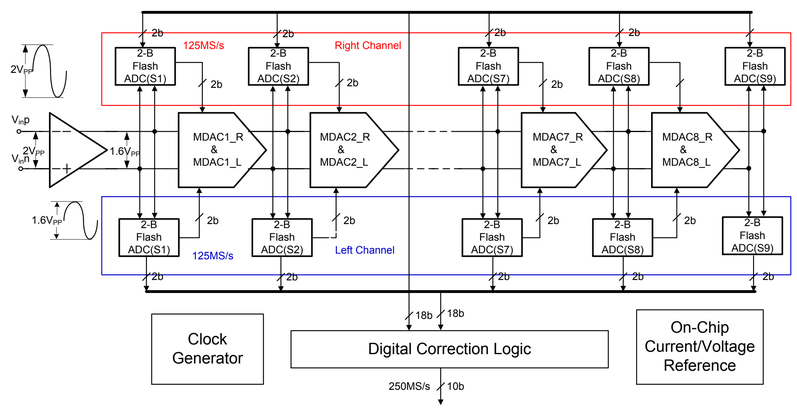
A Low-Power 10-bit 250-MS/s Dual-Channel Pipeline ADC in 0.18 µm CMOS

Xiaoke Wen[b], Qingjun Fan[a], Jinghong Chen[a,b], Yulang Feng[a], Yuxuan Tang[a], Zhiheng Zuo[a], Bozorgmehr Vosooghi[a], Datao Gong[c], Tiankuan Liu[c], and Jingbo Ye[c]
[a] *Department of Electrical and Computer Engineering, University of Houston, Houston, TX 77004, USA*
[b] *Department of Electrical Engineering, Southern Methodist University, Dallas, TX 75275, USA*
[c] *Department of Physics, Southern Methodist University, Dallas, TX 75275, USA*
xwen@mail.smu.edu, jinghong@uh.edu

Introduction

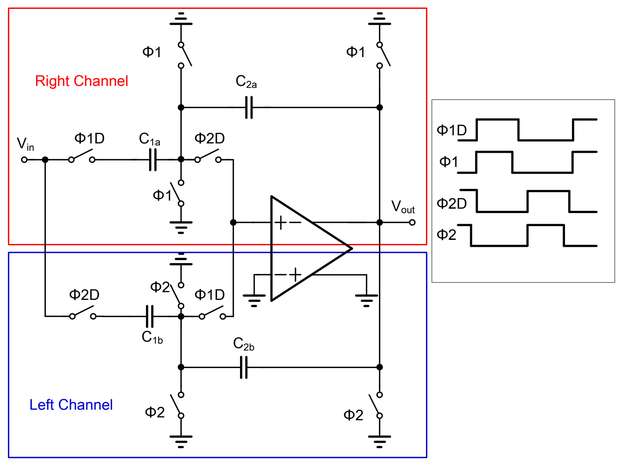
- High-resolution and low-power A/D converters are critical for multi-level modulations
- A 10-bit 250 MS/s low-power dual channel pipeline ADC is designed in 0.18µm CMOS technology
- To eliminate the sampling timing skew without using a calibration circuit, a unique clocking scheme that is applicable to bottom-plate sampling networks is adopted
- An opamp-sharing technique is proposed to reduce the power consumption without suffering from the memory effects
- The ADC achieves a maximum SNDR of 61.84 dB and a peak SFDR of 78.1 dB at 250 MS/s
- The ADC core consumes 32 mW of power under a 1.8-V power supply

Architecture

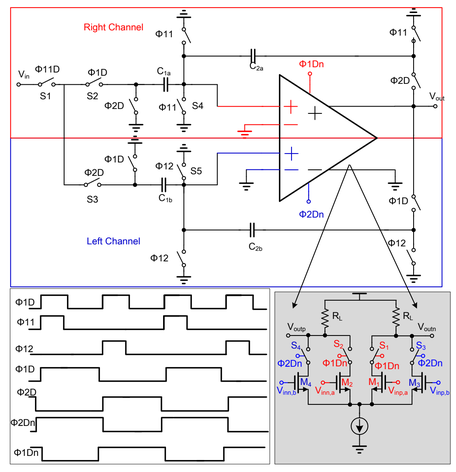


- A double sampled SHA shared by two time-interleaved channels, nine pipeline stages per channel including eight 1.5-bit per-stage MDACs and a 2-bit backend flash
- Opamps are shared between the two interleaved channels based on the proposed dual-input opamp-sharing MDAC to improve the ADC power efficiency

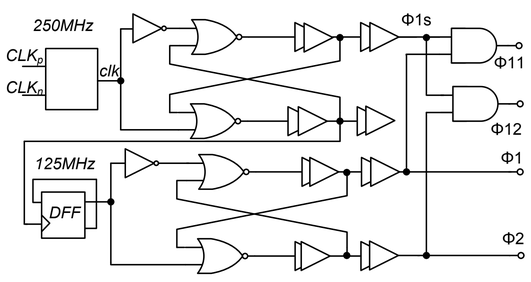
Double-Sampled SHA



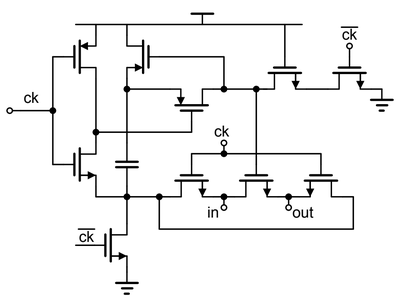
Conventional double-sampled SHA structure



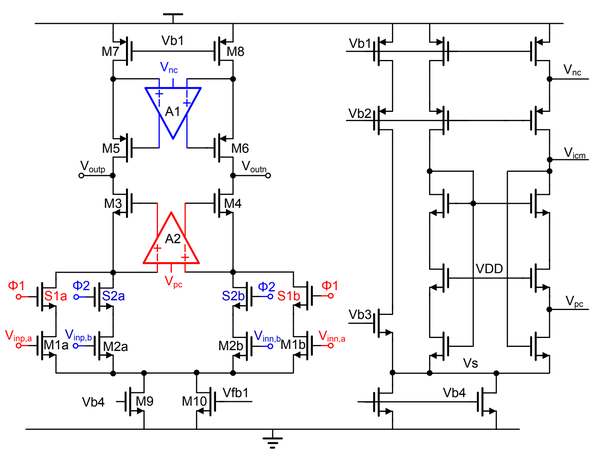
The proposed double-sampled SHA and the timing diagram



Proposed clock generation circuit

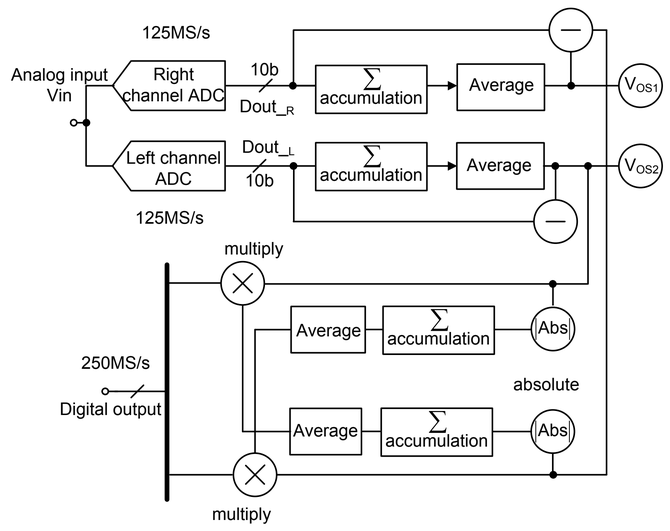


Bottom-plate sampling switch

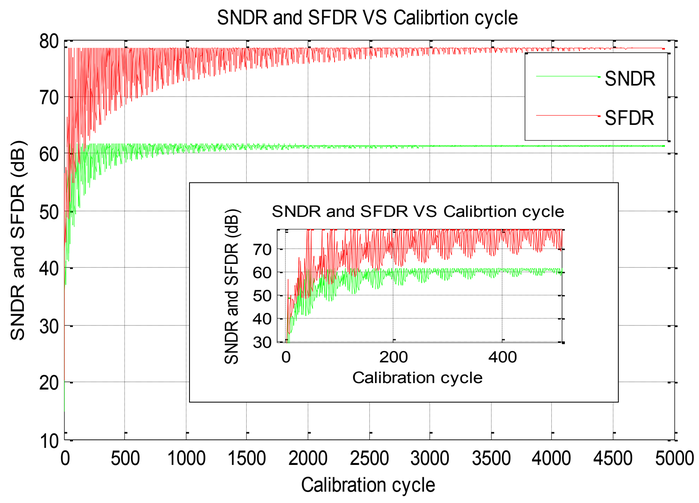


Shared opamp and bias circuit insensitive to the input common mode variation

Calibration



Block diagram of the gain and offset calibration algorithm



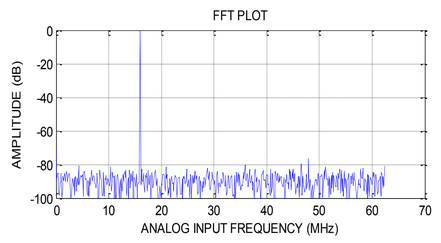
Convergence of the calibration process

ADC PERFORMANCE SUMMARY

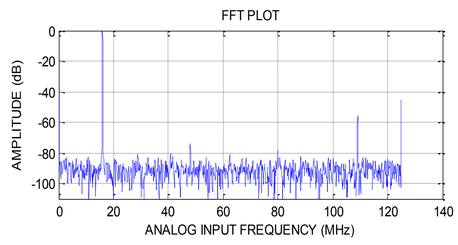
Technology	0.18-µm CMOS
Conversion Rate	250MS/s
Input Range	1.6Vpp
SNDR	61.84dB@17MHz input
SFDR	77.8dB@17MHz input 78.1dB@80MHz input 77.6dB@120MHz input
Power Consumption	32 mW
FOM (P/2^ENOB/Fs)	0.14pJ/step* (consider simulated Noise Floor)

- 0.18µm CMOS
- Conversion rate of 250 MS/s
- Input range of 1.6Vpp
- Maximum SNDR of 61.84 dB
- Peak SFDR of 78.1 dB
- Power consumption of 32 mW under 1.8V supply

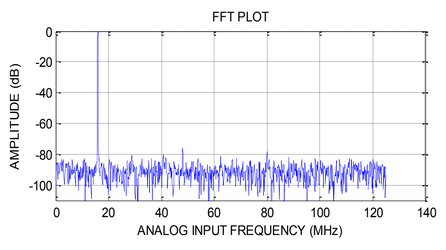
Simulated Performance



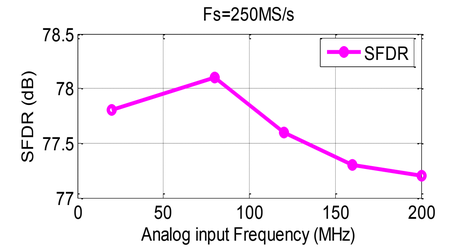
FFT spectrum of a single channel ADC



FFT spectrum of the dual channel ADC without calibration



FFT spectrum of the dual channel ADC with gain and offset calibration



SFDR vs input frequency

PERFORMANCE COMPARISON

Ref	VDD (V)	Fs (MS/s)	SFDR (dB)	SNDR (dB)	Power (mW)	FOM (pJ/step)
[1]	1.8	300	N/A	56.6	40	0.24
[2]	1.2	320	70	53	40	0.78
[3]	1.2	500	N/A	52.8	55	0.31
This work	1.8	250	78.2	61.8	32	0.14

Conclusion

- A 10-bit 250MS/s time-interleaved pipelined ADC with opamp-sharing using a unique timing scheme to eliminate the timing skew between channels is presented
- The pipeline ADC achieves an ENOB of 9.98 bits with a SFDR of 78.2 dB at 250MS/s and consumes 32mW of power under 1.8V supply

References

[1] M. Miyahara, H. lee, D. Paik, A. Matsuzawa,“A 10b 320 MS/s 40 mW open-loop interpolated pipeline ADC”, IEEE VLSI Circuits, 2011 Symposium on, pp 126-127, June 2011.
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[3] E. Alpman, H. Lakdawala, L. Carley, K. Soumyanath, “A 1.1V 50mW 2.5GS/s 7b Time-interleaved C-2C SAR ADC in 45nm LP Digital CMOS”, IEEE International Conf. of Solid-State Circuits, pp. 76-77, Feb. 2009.

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