A Low-Power 10-bit 250-MS/s Dual-Channel Pipeline ADC in 0.18 µm CMOS

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Introduction

- High-resolution and low-power ADC converters are critical for multi-level modulations.
- A 10-bit 250 MS/s low-power dual-channel pipeline ADC is designed in a 0.18um CMOS technology.
- To eliminate the sampling timing skew without using a calibration circuit, a unique clocking scheme that is applicable to bottom-plate sampling networks is adopted.
- An opamp-sharing technique is proposed to reduce the power consumption without suffering from the memory effects.
- The ADC achieves a maximum SNDR of 61.84 dB and a peak SFDR of 78.1 dB at 250 MS/s.
- The ADC core consumes 32 mW of power under a 1.8-V power supply.

Architecture

- A double sampled SHA shared by two time-interleaved channels, nine pipeline stages per channel including eight 1.5-bit-per-stage MDACs and a 2-bit backend Flash.
- Opamps are shared between the two interleaved channels based on the proposed dual-input opamp-sharing MDAC to improve the ADC power efficiency.

Double-Sampled SHA

- Conventional double-sampled SHA structure.
- The proposed double-sampled SHA and the timing diagram.

Calibration

- Block diagram of the gain and offset calibration algorithm.
- Converge the calibration process.

Conclusion

- A 10-bit 250MS/s time-interleaved pipelined ADC with opamp-sharing using a unique timing scheme to eliminate the timing skew between channels is presented.
- The pipeline ADC achieves an ENOB of 9.98 bits with a SFDR of 78.2 dB at 250MS/s and consumes 32mW of power under 1.8V supply.

Simulated Performance

- FFT spectrum of a single channel ADC.
- FFT spectrum of the dual-channel ADC without calibration.

References


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