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A Low-Power 10-bit 250-MS/s Dual-Channel Pipeline ADC in 0.18 µm CMOS

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This paper presents a 10-bit 250-MS/s time-interleaved pipelined ADC. A distributed clocking scheme is developed to eliminate timing skew between channels without introducing load capacitance to the driving buffer. The channel offset and gain mismatch error is calibrated in digital domain. In addition, a switch-embedded opamp-sharing technique is developed to reduce ADC power consumption and eliminate the memory effect. The simulated SNDR and SFDR are 61.84 dB and 78.2 dB, respectively. The ADC core consumes 28mW under a 1.8V supply at 250 MS/s sampling rate.

Summary

High-speed and radiation-tolerant ADC is widely needed for LHC upgrade and other collider detector developments. With continued scaling of CMOS technology, successive-approximation-register (SAR) ADC has recently become attractive for low-power medium-speed applications. However, for high-speed and high-resolution applications, pipeline ADC is still the most practical and cost effective solution. One of the key aspects in designing pipeline ADC is to achieve a high signal-to-noise and distortion ratio (SNDR) with good power efficiency.

Time-interleaved pipeline ADC is an effective approach to obtain both high-speed high-resolution and good power efficiency. This paper presents a 10-bit 250-MS/s dual-channel pipeline ADC. Each channel operates at 125 MS/s and consists of a sample-and-hold amplifier (SHA), eight 1.5 bit-per-stage MDACs, and a 2-bit flash ADC. The opamps of the SHA and MDAC are shared by the two channels utilizing a current-reused opamp-sharing technique. To reduce the ADC noise floor, a wider swing input signal (2Vpp) is used in the sampling network and then the input signal is attenuated to 1.6Vpp by the SHA to ensure the MDAC operate properly under the supply voltage of 1.8V. This improves the ADC SNR by reducing the noise contribution of the sampling network without suffering from the linearity degradation.

The time-interleaved pipelined ADC, however, exhibits offset and gain mismatch between channels and is sensitive to timing skew of the clocks distributed to them. The channel mismatch error is calibrated by obtaining the matched long-term mean and RMS values from the two channels and the calibration is based on a least-mean-square (LMS) scheme. To minimize the timing skew error, a single-edge distributed bottom-plate sampling network is developed. The sampling network ensures a precise symmetrical sampling clock that is also insensitive to clock duty cycle. To reduce the resistance of the switch in the sampling network, bootstrapped switch is used and an improved bootstrapped switch structure is developed to minimize the charge injection impact on the ADC performance. Furthermore, a switch-embedded opamp-sharing technique is developed to lower the ADC power consumption and to eliminate the memory effect.

The proposed 10-bit 250MS/s pipelined ADC is designed in a 0.18-µm CMOS technology. Simulation results show that the ADC core consumes 28mW of power under a 1.8V supply at 250 MS/s sampling rate. The simulated SNDR and SFDR of the ADC are 61.84 dB and 78.2 dB, respectively. The ADC will be submitted for fabrication in July and extensive electrical and radiation performance testing will be carried out. The testing results will be presented in the final paper.

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