Development of a Clock-Data Recovery circuit, Serializer and CML Driver in 65nm CMOS for HL-LHC pixel readout chips

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Motivation

The LHC Phase-II upgrade will lead to a significant increase in luminosity, which in turn will bring new challenges for the operation of the inner tracking detectors. In order to cope with the envisioned extreme rates (hit rate of 2 GHz/cm2, trigger rate of 1-2MHz) and radiation levels (500Mrad – 1Grad) ATLAS and CMS experiments are currently jointly developing a pixel readout chip to be used in the inner most layers of detectors (RD53 collaboration). The chosen technology is TSMC 65nm CMOS. This work presents three building blocks designed for the input/output interface of the mentioned readout chip: a clock-data recovery (CDR) circuit, a serializer (SER) and a cable driver.

Clock-Data Recovery Circuit

- Designed for a input data rate of 160 Mbps
- Four types of Phase Detector (PD) were implemented for performance and SEU hardness testing (Figure 1.)

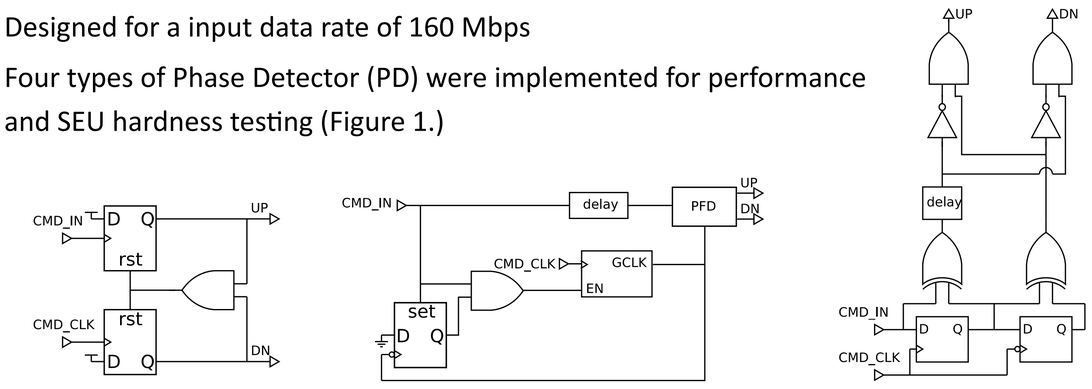

Figure 1. Schematics of implemented blocks: classical phase frequency detector (left), clock gating PD (middle), improved Hogge's detector (right).

- VCO based on differential buffers with cross-coupled loads (output frequency range: [0.5GHz, 3.5GHz] with default value of 1.6GHz)
- Four versions of dividers were implemented differing by division ration (8 or 10) and SEU protection scheme
- Full custom design including modified standard cells (resized for better radiation hardness)
- Simulation of RC-extracted circuit show jitter of VCO output of approx. 1ps rms (Figure 2) and power consumption of 3.6 mW
- Simulation of circuit using 200 Mrad corner shows no significant performance degradation (Figure 3)

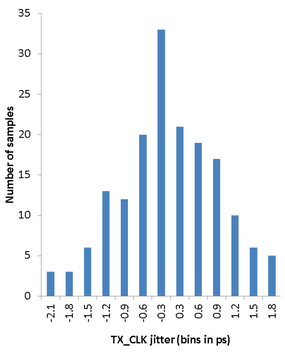

Figure 2. Histogram of VCO output jitter (locked at 1.6GHz)

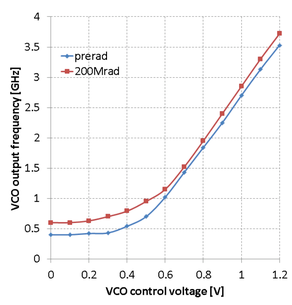

Figure 3. VCO frequency as a function of control voltage.

Serializer

- 20:1 serializer designed for 3.2Gbps output (DDR @ 1.6GHz)
- Composed of LOAD signal generator, 20 sampling DFFs and SER core (Figure 4)
- SER core based on DFF and MUX using double data rate architecture (Figure 5)

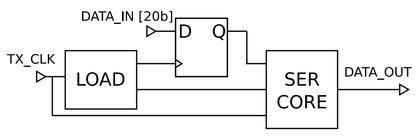

Figure 4. Simplified schematic of SER.

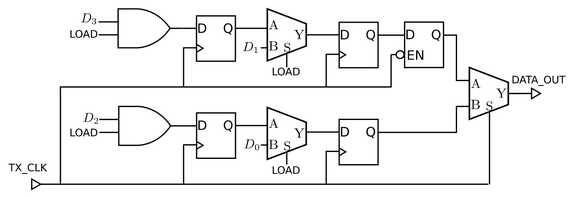

Figure 5. Simplified to 4:1 example of used architecture of SER.

- Four versions of LOAD signal generators were implemented for performance and SEU hardness evaluation (examples in Figure 6)

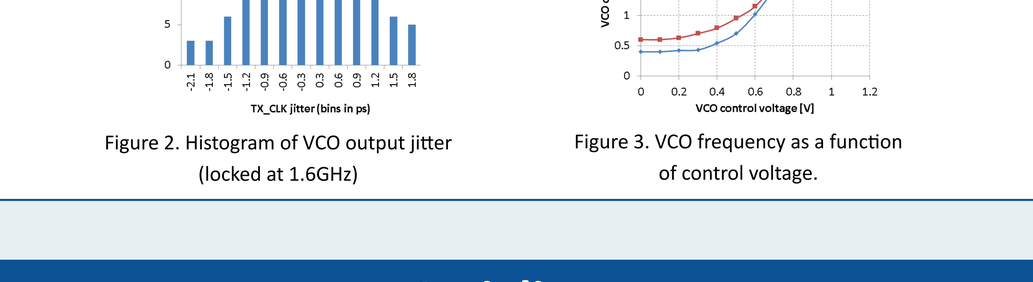

Figure 6. Diagrams of two implemented blocks: self resetting generator (left) and triplicated generator with counters (right).

- Design based on modified standard cells (resized for better radiation hardness)
- Power consumption ranges from 1.4mW to 4mW depending on SER type

CML Cable Driver

- Current Mode Logic driver based on nMOS only
- 3-tap architecture with adjustable tap width and weight (Figure 7)
- According to simulation capable of driving 2m of ultra low mass cable with 4Gbps rate (Figure 8)

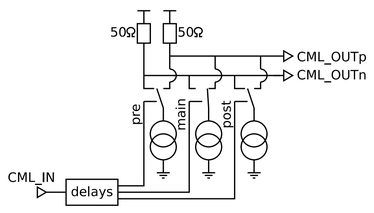

Figure 7. Schematic of CML driver.

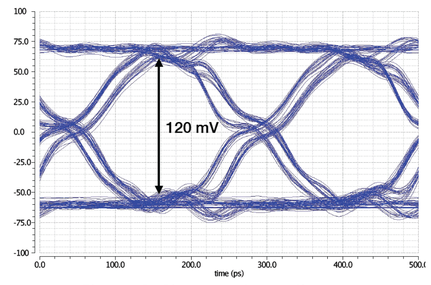

Figure 8. Simulated eye diagram (4Gbps, 2m of ultra low mass cable).

Test Chip

- Includes CDR, SER and CML driver
- Circuits connected in a way allowing characterization of each block separately and full chain CDR—SER—CML (Figure 9)
- Two power domains (1st: CDR + SER, 2nd: CML)
- Chip size: 1mm × 2mm (Figure 10)

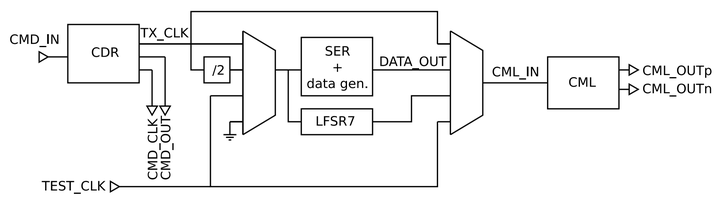

Figure 9. Diagram of blocks connections in the test chip.

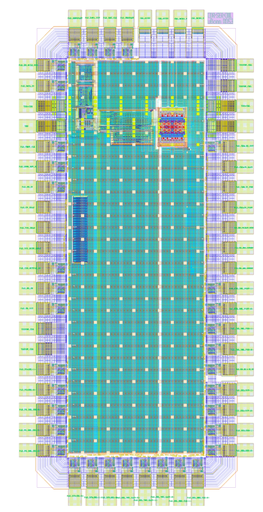

Figure 10. Layout of the test chip.

Preliminary measurement results

- Testbench consisting of MIO card (communication with PC), GPAC card (voltage and current sources) and chip carrier PCB (shown in Figure 11)

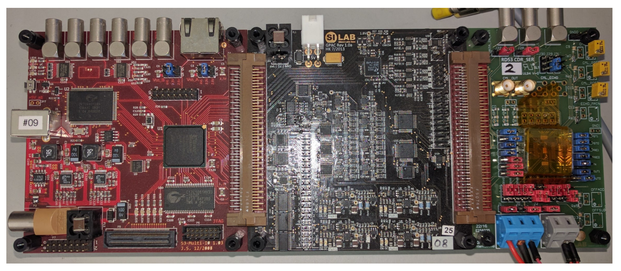

Figure 11. Testbench: MIO card (left), GPAC card (middle) and test chip carrier PCB (right).

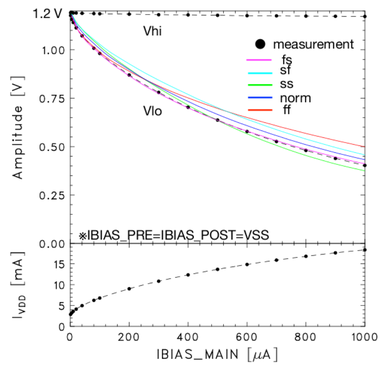

Figure 12. CML driver output level—comparison between measurement and simulation.

- Python based control software
- First test indicate that all block are operational
- Measurement results are in good agreement with fs corner (Figure 12)
- Full chain (CDR+SER+CML) works, output eye diagram (for 4Gbps) shows 24ps rms of jitter (Figure 12)
- CDR can stay locked with patterns including up to 32 consecutive 0's or 1's
- Further measurement and tuning needed
- After functional testing radiation and SEU hardness will be evaluated

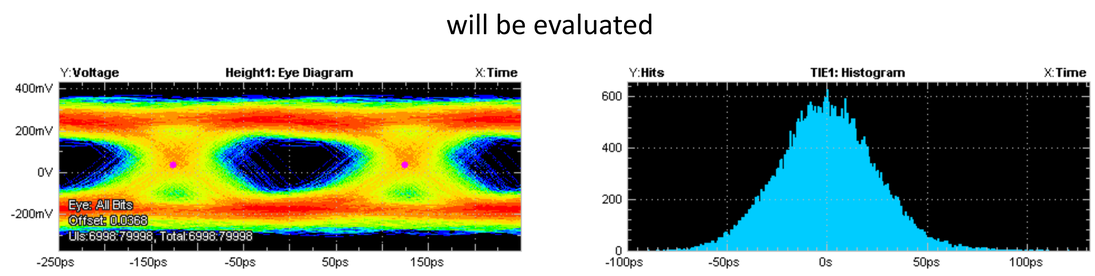

Figure 13. Preliminary results of CDR-SER-CML chain with output running at 4Gbps: eye diagram (left) and histogram of output jitter (right).

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