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Development of Clock-Data Recovery circuit, Serializer and CML Driver in 65nm CMOS for HL-LHC pixel readout chip

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ATLAS and CMS are presently collaborating on a design of a pixel readout chip in 65nm CMOS technology to be used for the LHC Phase-II upgrade. This work presents a prototype containing part of the I/O interface of this readout chip. The clock-data recovery circuit recovers clock from 160 Mbps incoming data and produces 1.6 GHz clock to be used by serializer. Double data rate serializer combines 20 data streams into 3.2Gbps stream, which is send off-chip by a Current Mode Logic driver. Prototype description together with first measurement results will be presented.

Summary

The LHC Phase-II upgrade will lead to a significant increase in luminosity, which in turn will bring new challenges for the operation of the inner tracking detectors. In order to cope with the envisioned extreme rates (hit rate of $2 \frac{GHz}{cm^2}$, trigger rate of 1-2MHz) and radiation levels (500Mrad –1Grad) ATLAS and CMS experiments are currently jointly developing a pixel readout chip to be used in the inner most layers of detectors. The chosen technology is TSMC 65nm CMOS. This work presents three building blocks designed for the input/output interface of the mentioned readout chip: a clock-data recovery (CDR) circuit, a serializer (SER) and a cable driver.

The CDR was designed to work with input data rate of 160Mbps. In addition to recovering clock from input data the CDR produces a 640MHz/800MHz/1.28 GHz/1.6GHz (depending on chosen configuration) fast clock signal that is used by serializer. This signal is an output of a Voltage Controlled Oscillator (VCO), which is based on differential buffers with cross-coupled loads. The gain of VCO can be adjusted to an appropriate value for any technology corner. The fast clock is divided down (by factor of 8 or 10) and fed to a Phase Detector (PD). Both the signal divider and PD were implemented in few flavours, differing by circuit architecture and SEU protection scheme. Output of PD is sent to a charge pump whose output is connected to the VCO input through second order passive low pass filter, thus completing the circuit loop. According to simulation a 550fs (rms) phase jitter of VCO output clock is achieved with a power consumption of 3.6mW (for default CDR configuration).

Double data rate serializer used in this prototype produces a 3.2 Gbps data stream out of 20 input streams. Circuit is based on two chains of D Flip-Flops and multiplexers working in parallel. Four flavours were implemented, differing by the SEU protection method. All of them were build out of modified standard cells, which provide improved radiation hardness. Power consumption varies from 1.4mW to 4mW, depending on a flavour.

Output driver is based on Current Mode Logic (CML) architecture. It provides programmable pre-emphasis (3-tap, with adjustable tap weight and width) and according to simulation is capable of transmitting 4Gbps signal across 2m of ultra-low mass cable.

Presented prototype was designed in a way that allows characterization of full chain (CDR-SER-CML) and each block separately. In this work the circuit will be presented in detail followed by simulation and measurement results.

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