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A Temperature Compensated Triple-path PLL for DUNE Experiments

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Many HEP applications require circuits to continuously operate over large temperature range. In particular, the DUNE experiment requires circuits be capable of operating at cryogenic temperature. We present a novel temperature-compensated triple-path PLL (TP-PLL) for this application. The TP-PLL is capable of automatically compensating its frequency as temperature changes while maintaining stable operation and good jitter performance. A prototype TP-PLL at 2.56GHz has been implemented using 65nm CMOS process. It occupies an area of 0.08 mm², consumes 13.2 mW, and has a frequency drift reduction by 99%.

Summary

Phase-locked loops (PLL) is a key circuit block in data links for High-Energy Physics (HEP) applications. Once started, the data links are required to work continuously with very low bit error rate over a wide operation temperature range. In particular, the DUNE experiments require data links be capable of continuously operating at cryogenic temperature of 77 K for 20-30 years.

We present a novel triple-path PLL (TP-PLL) that is capable of automatically compensating the VCO frequency drift over large temperature variations in a closed loop manner meanwhile maintaining stable bandwidth and low phase noise and jitter. The VCO in the presented TP-PLL has three control paths, the proportional path (PP), the integral path (IP), and the temperature compensation path (TCP). Each of the three paths employs its own varactor in the VCO LC tank for frequency tuning. First of all, the main PLL loop is split into two paths, the IP and the PP. Each of the PP and IP has its own charge pump and a portion of the loop filter: a resistor in the PP and a capacitor in the IP. The separation of the IP and PP allow for individual control on the gain of each path, resulting in well defined and almost fixed control voltage on the PP to maintain good phase noise of the VCO. Second, an auxiliary path, the TCP, is added to the main PLL loop. The TCP employs a large VCO gain (KVCOTMP) to effectively compensate for the VCO frequency drift over large temperature change. It consists of a gain stage and a low-pass filter, which detects and amplifies the voltage change on the main control path and based on this information tune the TCP varactor to compensate for the VCO frequency drift. Since the temperature compensation is done on the TCP loop, not the main loop, the bandwidth and stability of the PLL is kept intact. The separation of TC path from the PP and IP allows a very small VCO gain on the latter two, which is important to maintain low phase noise and spurs for the VCO and therefore low jitter performance of the PLL. In addition, the different gain settings on the PP and IP work as a capacitor multiplier, allowing for the implementation of a large loop filter capacitor using small silicon area.

A prototype chip utilizing the proposed trip-path architecture with a center frequency of 2.56 GHz was designed and fabricated in 65 nm CMOS technology. The VCO frequency temperature drift in the proposed TP-PLL is reduced by 99% around the center frequency. The TP-PLL chip occupies an area of 0.08 mm² and consumes 11 mA from 1.2 V supply voltage. The prototype chip was submitted for fabrication in Feb. 2016 and the measurement of the chip will be carried out in the summer of 2016 and results will be presented at the TWEPP conference.

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