A Fully Monolithic HV-CMOS Pixel Detector with a Time-to-Digital Converter for Nanosecond Time Measurements

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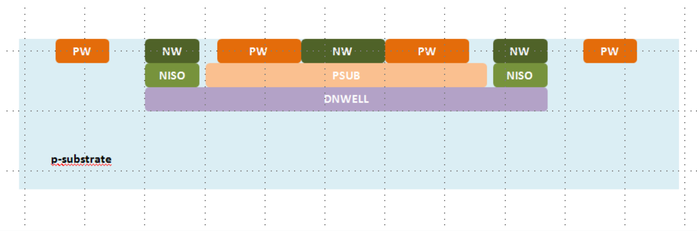
Introduction

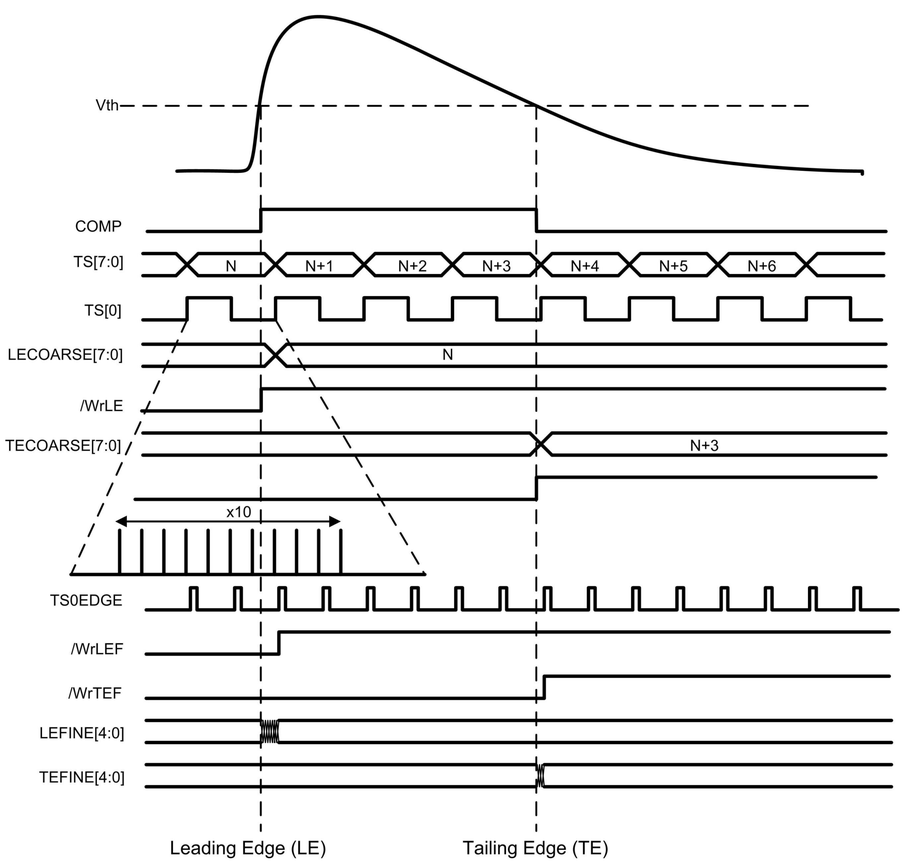
•Work done in the context of the RD50 collaboration
•Circuit designed to measure the Time of Arrival (ToA) and Time over Threshold (ToT) with nanosecond accuracy
•Depleted Monolithic Active Pixel Sensor. Two different pixels:
  •**50x50µm²**: analog front-end electronics on pixel, digital front-end electronics on the periphery
  •**75x75µm²**: analog and digital front-end electronics on pixel
•Sparse readout, only pixels with event information are readout
•Two main purposes:
  •Study the 150nm HV CMOS technology from LFoundry
  •Study full monolithic pixel with TDC on pixel

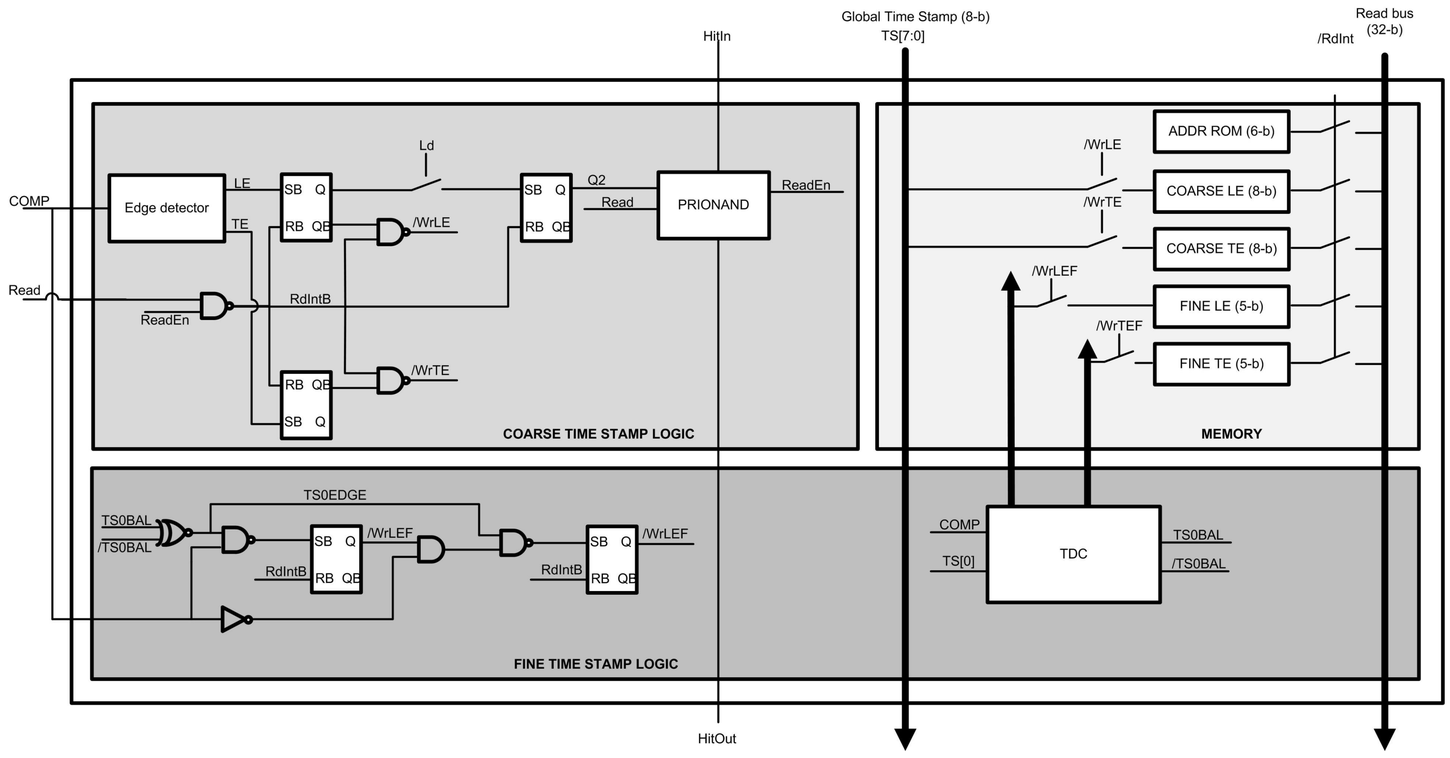
LFoundry technology

LFoundry 150nm process main features:
  •High voltage CMOS technology
  •Backside processing and stitching are possible
  •Extra isolation layer to avoid punch-through between n-wells inside a deep n-well. Integration of CMOS circuits on pixel



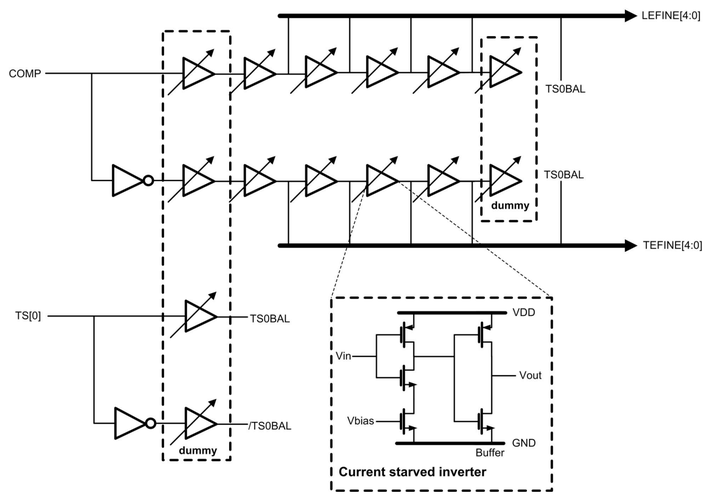
Overall architecture

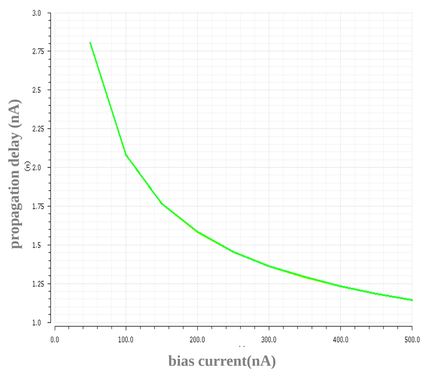




•Digital circuit that measures the time when the Leading Edge (LE) and Tailing Edges (TE) of the discriminator occurs
•ToT is calculated off-chip with the LE and the TE
•The nano-second accuracy is obtained by measuring the LE and TE in two steps:
  •**Coarse measurement**: capture of a 40-80MHz 8-bits global time stamp (LECORASE[7:0] and TECOARSE[7:0]). Digital electronics similar to FEI3.
  •**Fine measurement**: the clock period of the time stamp is divided into 10 equal time intervals by a TDC (LEFINE[4:0] and TEFINE[4:0])
•The pixel electronics includes:
  •**Analog front-end stage**: CSA + discriminator. Included on pixel.
  •**Digital front-end electronics**: electronics for coarse and fine time measurement. Either on pixel or periphery.
•Dynamic SRAM memories for timing storage (26-bits)
•Pixel address hardwired (ROM)
•Hit flag. Priority encoder (AND/OR)
•End of column includes a column time stamp generator and electronics to readout the time measurements and the address of the read pixel
•Readout done as in H35DEMO ASIC

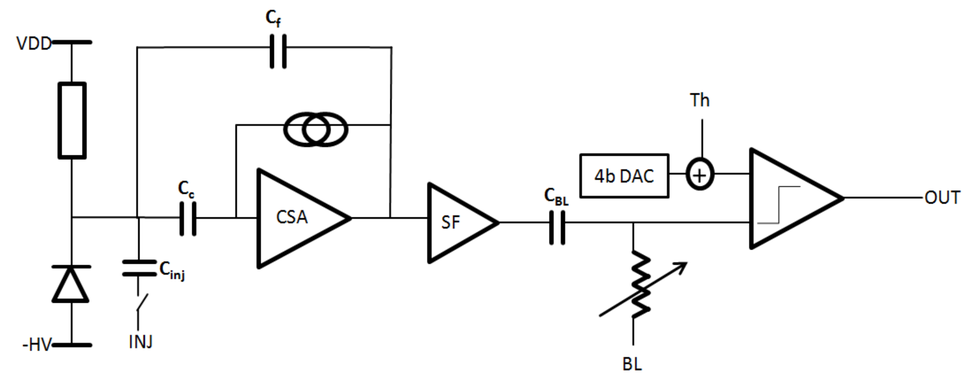
Time to digital converter

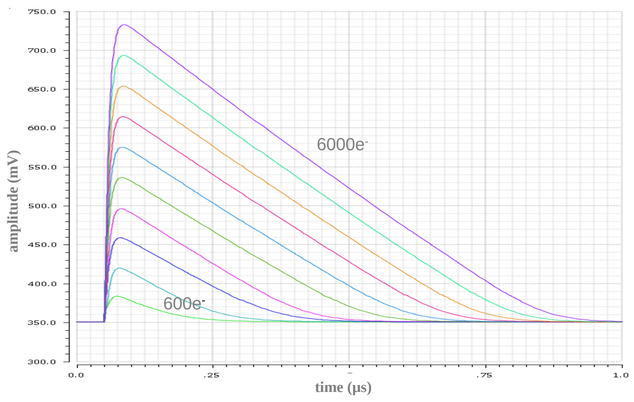




•TDC based on Delay Elements (DE) instead of oscillators in order to reduce cross talk on pixel
•Current starved inverter as DE
•Propagation time tunable by adjusting the bias current of the DE: 1ns-3ns
•Power consumption depends on the propagation time:50nA-400nA per DE.
•Delay line composed of two branches, one for LE measurement and the other for TE
•The DE are adjusted as a function of the clock period of the global time stamp
•Half a period is divided into five equal interval times by 4 DE (4-bits)
•The level of the clock signal is used as an additional bit. It indicates in which half a period of the clock the event occurred.

Analog front-end electronics





•Current Sense Amplifier based on a single folded cascode amplifier
•Base Line (BL) adjustable externally
•Global threshold voltage
•4-b DAC to adjust locally the threshold voltage
•Test pulse circuit

Main features	
Voltage supply	1.8V
Power consumption	< 54µW
Rise time	12ns
ENC	< 140e⁻
Area	38µm x 22µm