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A Fully Monolithic HV-CMOS Pixel Detector with a Time-to-Digital Converter for Nanosecond Time Measurements

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The Time Over Threshold (TOT) is usually measured by counting the number of clock cycles that the output of the preamp is over the threshold but the time resolution obtained is limited by the clock frequency and power consumption. Future HEP experiments will require a time resolution of few nanoseconds so that new approaches are needed. This paper presents a circuit to measure the TOT with a Time-to-Digital Converter (TDC). The circuit is very compact, low power and used to readout a matrix of HV-CMOS pixels. The chip is designed with a 150nm process from LFoundry.

Summary

HV-CMOS sensor technologies in several different commercial vendors are being developed to study which one offers the best features to suit the High Luminosity-LHC (HL-LHC) ATLAS upgrade. There is a special interest on the 150 nm HV-CMOS technology from LFoundry because allows backside processing and stitching. Moreover, it provides an extra isolation layer to avoid punch-through between an n-well nested inside a deep n-well. This feature allows the integration of CMOS comparators and even digital electronics inside the pixel area. To study this technology, a submission through an MPW is scheduled for July 2016. The reticle is fabricated in 2 different substrate resistivities: 1k Ω·cm and 2k Ω·cm. It has an area of 1 cm x 1 cm and is split in 3 regions to prove different ideas, not only for ATLAS but also for other experiments like the Mu3e. One of these regions has a total area of 0.25 cm x 1 cm and includes a matrix with a new pixel type that provides a time resolution in the nanosecond range.

The proposed solution measures with resolution of nanoseconds when the preamp output crosses above and below the threshold level instead of measuring the number of clocks that the output is over the threshold. The two times, t1 and t2, are subtracted off-line to measure the TOT. The nanosecond resolution is obtained by using a global time stamp to determine t1 and t2 coarsely. A Time-to-Digital Converter (TDC) divides the period of a time stamp in 10 equal time intervals in order to give a fine measure of the time. It is composed of chain of Delays Elements (DE) instead of a ring oscillator in order to minimize the power consumption. The DE are tuneable in order to adjust the introduced delay to the time stamp period. The TDC produces a 5bits number. The most significant bit indicates in which half of the time stamp period the event occurred and the less fourth the in which of the 5 subintervals.

The analog front-end electronics are integrated into the pixel and include a preamp and a comparator. There are two versions of the analog part, one includes a fully CMOS comparator and the other one a comparator made of only NMOS transistors. The purpose is to study the performances of the isolation layer. The output of the comparator is sent to a digital ReadOut Cell (ROC) placed at the periphery. It is similar to the digital readout cell of the FEI3 chip, that is, it includes an event detector, a priority encoder and the address is hardwired. When a hit is detected, the ROC stores an 8 bit global time stamp and simultaneously activates the TDC to measure the time finely. The operation is repeated when the output of the preamp crosses below the reference level of the comparator. A complete description of the circuit and its operation will be presented at the conference.

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