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Front-End and Back-End Solutions in the CBM STS Readout ASIC

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STS-XYTER2 is a new full-size CBM Silicon Tracking System and Muon Chamber prototype readout ASIC designed in UMC 180 nm CMOS technology. It is a self-triggered amplitude and time measurement chip implementing a digital back-end compatible with a GBTx-based data acquisition scheme with scalable data bandwidth. We present details on the front-end and back-end solutions used in this ASIC and simulation results.

Summary

We present the architecture of the STS -XYTER2 ASIC, a full-size, 128-channel prototype chip for the Silicon Tracking System (based on double-sided silicon strip sensors) and Muon Chamber (gas sensors) detectors at the Compressed Baryonic Matter experiment at FAIR, Germany. The charge processing channel includes a charge sensitive amplifier, shaper amplifiers forming two signal paths for timing measurement via a fast discriminator and low-noise amplitude measurement by a 5-bit continuous-time ADC with digital peak detector and is required to operate at average rate of 250 kHit/s/channel. Different operating conditions (including environment) and constraints of two target applications required flexibility and careful design to meet extended system-wise requirements. The circuit implements switchable shaper peaking time, gain switching and trimming, pulsed reset of the amplifier for increased input charge rate and faster recovery from overload, fail-safe measures and diagnostic modes for wafer-level and in-system testing and calibration. The chip required a robust and effective hit data streaming and control mechanism. The back-end implements fast channel readout, timestamp-wise hit sorting and data streaming via scalable interface implementing a dedicated protocol (STS-HCTSP) for chip control and hit transfer with data bandwidth from up to 47 MHit/s. It also includes options for link diagnostics, failure detection and throttling features. The chip is designed to operate within a GBTx-based data acquisition scheme.

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