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LDQ10P: A Compact Low-Power 4x10 Gb/s VCSEL Driver Array IC

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Low-power and high-data-rate laser array driver is an important on-detector component of the Versatile Link for the high-luminosity LHC experiments. We report the design and implementation of a low-power and radiation-tolerant 4x10 Gb/s VCSEL Driver array IC (LDQ10P). The entire four-channel VCSEL driver consumes 130 mW and occupies a silicon area of $1900\ \mu\text{m} \times 1700\ \mu\text{m}$. By integrating four driver channels into a single chip, LDQ10P can be directly wire-bonded to the VCSEL array and is a suitable candidate for the Versatile Link.

Summary

Low-power, high-speed and radiation-tolerant Gigabit data links are needed for data transmission in High-Energy Physics (HEP) applications. Last year we reported and demonstrated a low-power 10 Gb/s single-channel laser driver IC (GBLD10P) implemented in 65 nm standard CMOS technology, with 40 mW power consumption at 10 Gb/s.

In this work, we present a 4x10 Gb/s low-power VCSEL driver array (LDQ10P) IC with compact chip size suitable to drive a VCSEL array. Each channel in the LDQ10P consists of a high-speed limiting amplifier (LA) and an output driver with programmable pre-emphasis. To fit the design in a compact silicon area, the LA employs a two-stage differential amplifier but with only one peaking inductor ($130\ \mu\text{m} \times 130\ \mu\text{m}$) shared between the two stages, boosting the driver speed without the area penalty that would be required by a conventional inductive-peaking LA. In the output driver stage, the feed-forward topology is adopted to further enhance the bandwidth. The feed-forward strength is carefully optimized trading-off between bandwidth and jitter. Moreover, to compensate for potentially slow tail speed of the laser devices and/or accommodate different packaging and load parasitics, an edge-dependent pre-emphasis is implemented in LDQ10P with three possible configurations, rising-edge pre-emphasis, falling-edge pre-emphasis and both-edge pre-emphasis. Compared to our published single-channel 10 Gb/s driver, the design is further optimized to obtain higher bandwidth and lower jitter. The total jitter is expected to be less than 15 ps with PRBS7 at BER of 10⁻¹².

The LDQ10P die size is $1900\ \mu\text{m} \times 1700\ \mu\text{m}$ and the entire chip consumes 130 mW (including the I2C block) when setting four VCSELs with 4 mA modulation and 6 mA bias current. Two on-chip 7-bit DACs are used to program the modulation and bias currents with a current resolution of 0.16 mA and a range of 10 mA radiation-hard and single-event immune I2C digital circuit is designed to control the IC operation. The driver array has a pitch of $250\ \mu\text{m}$, compatible with that of the VCSEL array devices. These features allow the IC to be directly wire-bonded to a VCSEL array. To minimize the crosstalk between the channels, extensive simulations and layout optimization including carefully designed power mesh and decoupling capacitor network were conducted. The LDQ10P prototype chip design has been submitted for fabrication in March, 2016. The chip measurement will be carried out during the summer of 2016 and the measurement results will be presented at the TWEPP conference.

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