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Simulation Environment Based on the Universal Verification Methodology

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This talk presents Universal Verification Methodology (UVM) simulation environments of three recent ASIC and FPGA projects, which have successfully implemented a new Coverage-Driven Verification (CDV) workflow in System Verilog: (1) the CLICpix2 65 nm CMOS hybrid pixel readout ASIC design; (2) the C3PD 180 nm High-Voltage-CMOS active sensor ASIC design; (3) the FPGA-based DAQ system of the CLICpix chip. Different interfaces (Ethernet, trigger and timing interface, I2C, SPI) which stimulate the devices under test are handled by complex and versatile testbenches enabling an exhaustive system verification and identification of difficult-to-track design flaws.

Summary

The Universal Verification Methodology (UVM) is a standardized approach of verifying integrated circuit designs, targeting a Coverage-Driven Verification (CDV). It combines automatic test generation, self-checking testbenches, and coverage metrics to indicate progress in the design verification. The flow of the CDV differs from the traditional directed-testing approach. With the CDV, a testbench developer, by setting the verification goals, starts with an structured plan. Those goals are targeted further by a developed testbench, which generates legal stimuli and sends them to a device under test (DUT). The progress is measured by coverage monitors added to the simulation environment. This way, the non-exercised functionality can be identified. Moreover, the additional scoreboards indicate undesired DUT behaviour. This talk presents the simulation environments of three recent ASIC and FPGA projects which have successfully implemented the new workflow and serve as examples of the UVM and System Verilog usage: (1) the CLICpix2 65 nm CMOS hybrid pixel readout ASIC design; (2) the C3PD 180 nm HV-CMOS active sensor ASIC design; (3) the FPGA-based DAQ system of the CLICpix chip. Different interfaces (Ethernet, trigger and timing interface, I2C, SPI) which stimulate the DUTs are handled by a complex and versatile testbenches enabling an exhaustive system verification and identification of difficult-to-track design flaws.

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