SPIDR

a General-Purpose Readout System for Pixel ASICs

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SPIDR Overview

The SPIDR Readout System is a flexible general-purpose readout platform for new and existing pixel (or other) ASIC projects. The system consists of an FPGA board, which reads out the ASIC and communicates via 1 and 10 Gigabit Ethernet to the back-end DAQ/PC. The Medpix3, Timepix3 and VeloPix are currently supported. SPIDR can be easily adapted and used as a test-bed for other ASIC's.

The Ethernet interfaces handle the connection to the back-end. These can be used simultaneously for high speed data and configuration/slow control over separate channels.

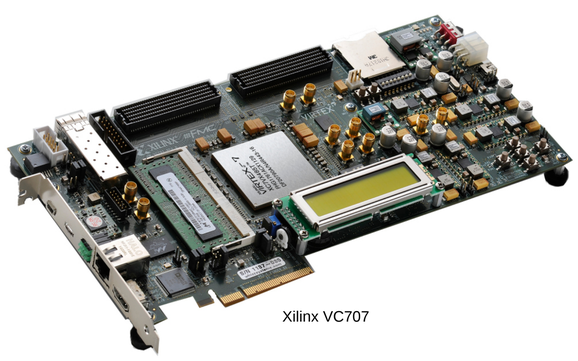
The gap between an ASIC and the data acquisition back-end is bridged by the SPIDR system. Using the FMC connector as an interface, only a simple chip carrier PCB is required.

SPIDR Hardware

The SPIDR system is based on the Xilinx 7-series FPGA's. This allows a wide range of devices that can be used in a readout with minimal changes. Currently the SPIDR firmware is built for the Virtex 7 (XC7VX485T) FPGA on the Xilinx VC707 development board and the Atrix 7 (XC7A200T) FPGA on the Compact SPIDR board.

Xilinx VC707 Development board

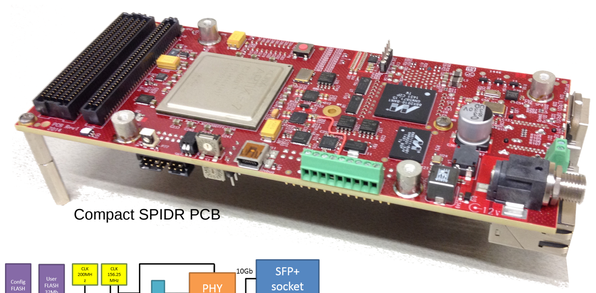
The VC707 development board is an “off the shelf” component.
It can read out 2 Timepix3 chips at full speed using both FMC connectors.



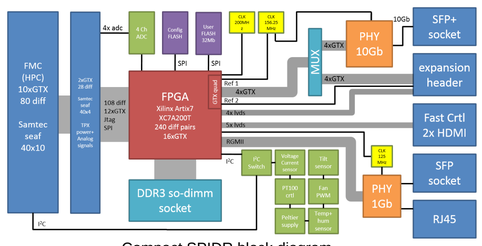
Xilinx VC707

SPIDR Compact

The SPIDR compact PCB was designed at Nikhef to fulfill the need for a more portable system. The board is still based on the FMC connector standard and a Xilinx 7-series FPGA, allowing compatibility with the VC707 board. Apart from the size the Compact SPIDR board has more dedicated functionality for this application, like dedicated power lines and sensors.



Compact SPIDR PCB

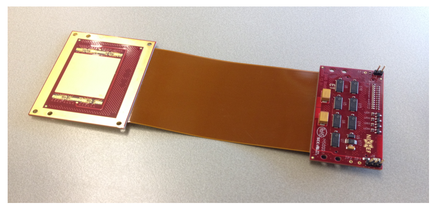


Compact SPIDR block diagram

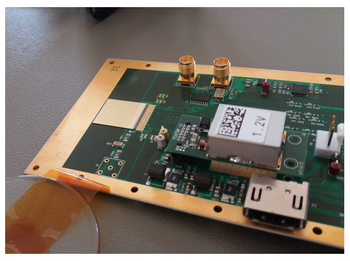
Chip boards

For the various project different chip boards were produced.
These range form “simple” single chip boards to advanced “flex-rigid” designs like the Timepix3 quad board

Timepix3 single chip board



Timepix3 quad chip board



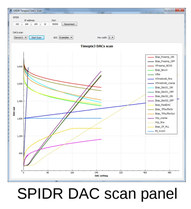
VeloPix chipboard

SPIDR software API

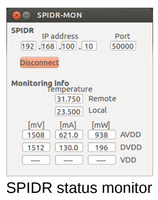
For the SPIDR system an “Application programming interface” (API) was written to control the SPIDR system on the PC side. Using this API, commands can be transmitted and received over a TCP/IP Ethernet link.
The API also provides the Data Acquisition (DAQ) classes to receive the high speed stream of UDP packets.
The API controls both the SPIDR board and the ASIC’s. A large part of the API can therefore be reused for other ASIC’s.
Using the API, “simple” programs can be written like a DAC panel or threshold equalization routine. The LEON3 CPU can handle multiple connections over TCP/IP simultaneously. Integration in larger DAQ or experiment control systems is also possible with this API.

```
#include "SpidrController.h"
#include "tpx3defs.h"

int main( int argc, char *argv[] )
{
  // Open a control connection to SPIDR-TPX3 module with address 192.168.100.10
  // on (default) port number 50000
  SpidrController spidrctrl( 192, 168, 100, 10 );

  // Are we connected to the SPIDR-TPX3 module?
  if( !spidrctrl.isConnected() ) {
    std::cout << spidrctrl.ipAddressString() << ": "
              << spidrctrl.connectionStateString() << ", "
              << spidrctrl.connectionErrString() << endl;
    exit(1);
  }

  int device_nr = 0;

  // Set some Timepix3 DACs
  int dac_val = spidrctrl.dacMax( TPX3_VTHRESH_COARSE ) / 4; // Set to 1/4th of max
  spidrctrl.setDac( device_nr, TPX3_VTHRESH_COARSE, dac_val );
  spidrctrl.setDac( device_nr, TPX3_VTHRESH_FINE, 0 );

  // Create and upload a Timepix3 pixel configuration
  spidrctrl.resetPixelConfig();          // Reset all to zero:
                                         // testpulse disabled, not masked, threshold=0
  spidrctrl.setPixelMask( 34 );          // Mask pixel column 34
  spidrctrl.setPixelConfig( device_nr );  // Upload the pixel configuration

  // Set Timepix3 acquisition mode
  spidrctrl.setGenConfig( device_nr, TPX3_POLARITY_EMIN | TPX3_ACQMODE_TOA_TOT );
  // Start acquisition
  spidrctrl.datadrivenReadout();
}
```

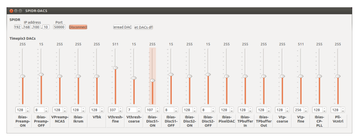
Example of the API usage



SPIDR DAC scan panel



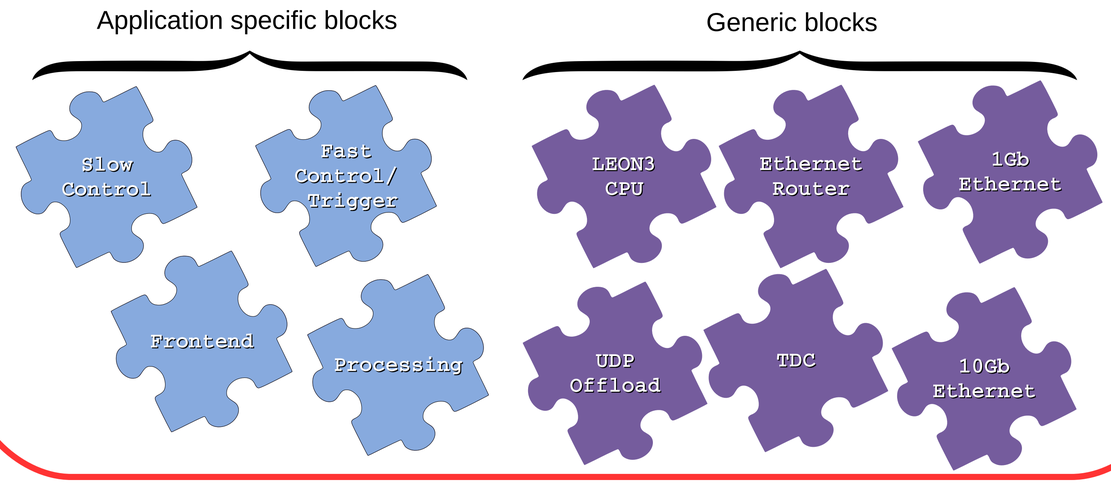
SPIDR status monitor



DAC panel for Timepix3

SPIDR Building blocks

The SPIDR firmware consists of a combination of several building blocks.
These blocks can be VHDL or VERILOG code performing different tasks.
For new designs the generic blocks can be reused and only the application / ASIC specific block have to be rewritten



Current and future applications

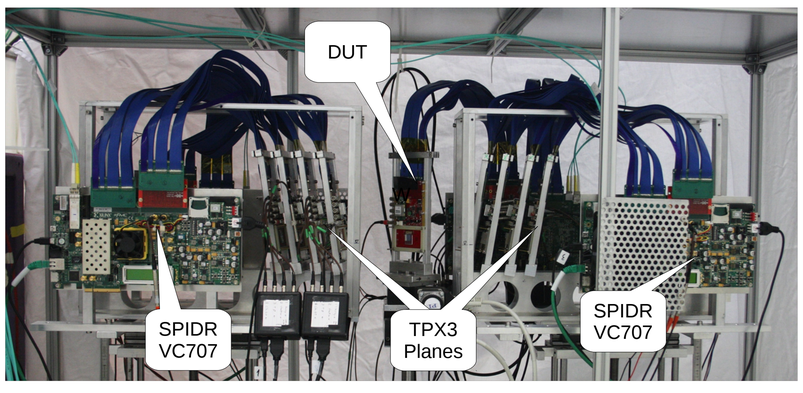
Timepix3 and Medipix3 compact readout system

- 1X Timepix3 at 80 Mhit/s
- 4X Timepix3 at 32 Mhit/s } “Data-driven” 1,6ns TOT+TOA
- 4X Medipix3 at 1.3K frames/s “Color” X-ray imaging
- 1 and 10Gb Ethernet connection
- Advanced internal and external trigger options
- Portable design
- Available for Medipix collaboration members
- Available for commercial party's trough Amsterdam Scientific Instruments (ASI)

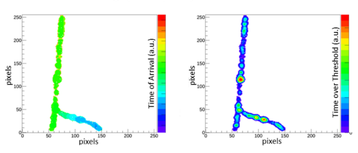
AMSTERDAM SCIENTIFIC INSTRUMENTS

LHCb Beamtelescope

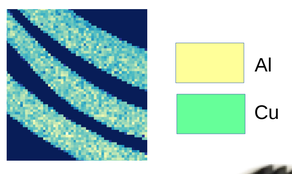
- Used for sensor characterization
- Operational since 2 years
- Readout of 8+dut Timepix3 chips
- Based on the VC707 development board
- Up to 10 million tracks/s in data-driven readout mode

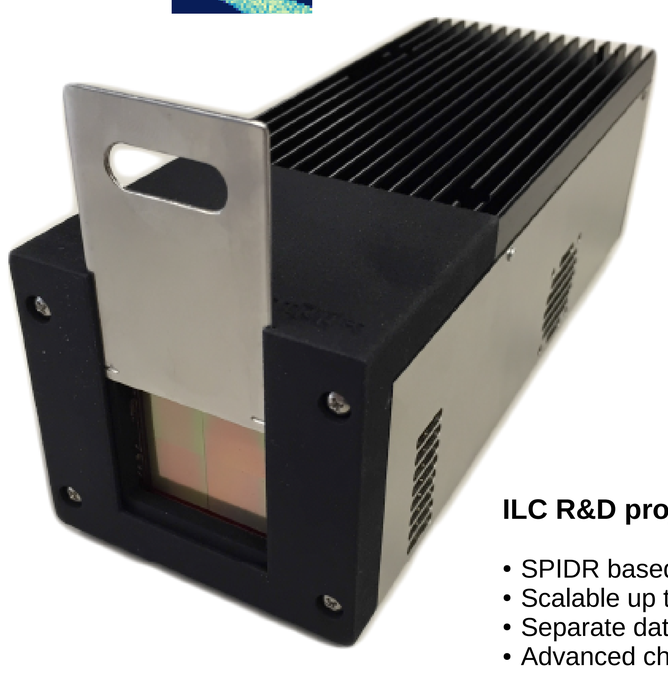


Particle Tracking (Timepix3)



Material recognition (Medpix3)

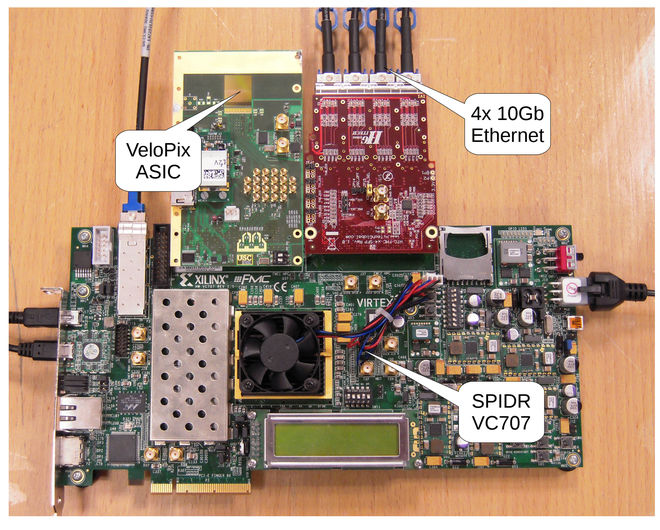




Compact SPIDR system

LHCb VeloPix testbed

- Readout of 1 VeloPix at full (20Gb/s) speed
- Based on VC707 development board
- Readout designed in parallel with ASIC design



ILC R&D project for a large area TPC (LEPCOL)

- SPIDR based readout of a large area Time Projection Chamber
- Scalable up to 128 Timepix3 chips per SPIDR @ 1 Mhit/s rate per chip
- Separate data concentrator to combine data of 16 chips to 1 high speed serial link
- Advanced chipboard under development, integrating: tiling, gas-seal and High voltage