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SPIDR, a General-Purpose Readout System for Pixel ASICs

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The SPIDR system is a flexible general-purpose readout platform for new and existing R&D ASIC projects, like Medipix3 and Timepix3. The system consists of an FPGA board, which reads out the ASIC and communicates via 1 and 10 Gigabit Ethernet to the back-end DAQ. It can be easily adapted and used as test-bed for other ASICs . The SPIDR system is currently used in various hybrid pixel detector projects such as the LHCb VeloPix. In this presentation we will highlight the architecture of the system and show a few successful applications of the SPIDR system.

Summary

The SPIDR system is a flexible general-purpose readout platform that can be easily adapted to test and characterize new and existing detector readout ASICs. It is originally designed for the readout of pixel ASICs from the Medipix/Timepix family, but other types of ASICs or front-end circuits can be read out as well.

The SPIDR system consists of an FPGA board with memory and various communication interfaces, FPGA firmware, CPU subsystem and an API library on the PC. The FPGA firmware can be adapted to read out other ASICs by re-using IP blocks. The available IP blocks include a UDP packet builder, 1 and 10 Gigabit Ethernet Mac's and a 'soft'CPU. Currently the firmware is targeted at the Xilinx VC707 development board and at a custom board called compact-SPIDR. The firmware can easily be ported to other Xilinx 7 series and ultra scale FPGAs.

The gap between an ASIC and the data acquisition back-end is bridged by the SPIDR system. Using the high pin count FMC connector only a simple chip carrier PCB is required. A 1 and a 10 Gigabit Ethernet interface handle the connection to the back-end. These can be used simultaneously for high-speed data and configuration over separate channels. In addition to the FMC connector, configurable inputs and outputs are available for synchronization with other detectors. A high resolution Time to Digital converter is provided for time stamping events in the detector.

The SPIDR system is frequently used as readout for the Medipix3 and Timepix3 ASICs. Using the 10 Gigabit Ethernet interface it is possible to read out a single chip at full bandwidth or up to 12 chips at a reduced rate. Another recent application is the test-bed for the VeloPix ASIC, which is developed for the vertex detector of the LHCb experiment. In this case the SPIDR system processes the 20 Gbps scrambled data stream from the VeloPix and distributes it over four 10 Gigabit Ethernet links, and in addition provides the slow and fast control for the chip.

In this presentation we will highlight the architecture of the system and show a few successful applications of the SPIDR system.

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