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The ARAGORN Front-End - FPGA Based Implementation of a Time-to-Digital Converter

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We present the ARAGORN front-end, a cost optimized, high-density Time-to-Digital Converter (TDC) platform. Four Xilinx Artix-7 FPGAs implement 384 TDC channels with a time resolution smaller than 200 ps on a single module. A fifth FPGA acts as data concentrator and master of an onboard SFP+ and a multi-channel optical transceiver slot to interconnect with up to seven boards though a star topology. This novel approach makes it possible to read out in total eight boards yielding 3072 input channels via a single optical fiber at a bandwidth of 6.6 Gb/s.

Summary

The ARAGORN board comprises four low cost Xilinx Artix-7 FPGAs out of the most recent device family in order to implement the TDC functionality of 384 differential input signals received by four Samtec QMS 208-pin high-speed connectors. The board comprises both a SFP+ optical transceiver module for data readout and an optional CXP transceiver slot. The optical interfaces are attached to the high-speed transceiver tiles of a fifth Artix-7 FPGA which in turn acts as data concentrator device for the TDC-FPGAs. This feature makes up an interconnection with up to seven boards as satellites using an optical fanout cable. Thanks to the pluggable implementation of the CXP transceiver module, the identical front-end layout is maintained independent of the final application.

The TDC application requires the sampling clocks of all front-ends recovered from the high-speed serial links to be phase-synchronous. Control signals have to be distributed with fixed latency to the receiver nodes in order to synchronize system timing. Special care was taken in the configuration of the integrated high-speed transceivers so that system synchronization is guaranteed upon repeated device initializations. Hence a challenge of the design is the jitter attenuation of the recovered clocks with deterministic output clock phase to replicate the uplink data among the CXP transceiver channels.

We decided to implement a shifted-clock sampling algorithm. Thereby, each TDC input channel is linked to a set of eight flip-flop components driven by equidistant phase-shifted clocks running at 311.04 MHz. Time stamps are encoded from the register output and accomplished by a coarse counter. The design allows the user to choose between rising, falling or both edge sensitivity during operation. The readout process is dead-time free with a double hit resolution limited by the sampling clock period. Reducing the overall data rate, a trigger signal can be used to further distinguish the physics events from background. For this purpose, the design includes an algorithm to pass only hits matching a given time window with respect to the trigger arrival time to the output FIFOs.

In conclusion, we present a highly versatile TDC platform with outstanding high-speed optical readout capabilities, strongly reducing the readout expenses. This novel approach permits 3072 input channels to be concentrated and read out with a single optical fiber at a bandwidth of 6.6 Gb/s. Another highlight is the superior channel density of a single module with a form factor of 140 mm x 172 mm comprising 384 TDC inputs, limited only by connector spacing constraints. Accordingly, we succeeded in the development of a very cost optimized design. The TDC implementation maintains a time resolution smaller than 200 ps for all channels using only 16 % of the flip-flop registers and 22 % of the look-up tables (LUTs) of the Artix-7 FPGA device resources. This will allow for FPGA design upgrades if future applications demand for even higher time resolution.

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