Versatile ASIC and Protocol Tester for STS/MUCH-XYTE2 in CBM Experiment

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Introduction
The Compressed Baryonic Matter (CBM) experiment is one of the experiments prepared at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt. Its main aim is the exploration of the QGP phase diagram in the region of high baryon densities during high-energy heavy-ion collisions. The CBM will utilize various particle detectors: Micro Vertex Detector (MVD), Ring Imaging Cherenkov Detector (RICH), Transition Radiation Detector (TRD), Time of Flight Detector (TOF), Projectile Spectrometer Detector (PSD), Silicon Tracking System (STS), Muon Detector (MD) (MUCH). The STS system for two of them - STS and MUCH - will be based on the dedicated ASIC - STS/MUCH-XYTE2.

STSMUCH-XYTE2

The STSMUCH-XYTE2 [2] is an ASIC implemented in CMOS technology, which measures both the charge produced by the converted detector in 128 input channels (with 5-bit resolution) and the incident to the STS/MUCH-XYTE2 offers also 58 output files for the configuration of the chip and the analog front-end (AFE) [3, 4]. Transmission of the measurement data and configuration commands is provided by the serial multiplex data communication interface using AC coupled LVDS interfaces, and the final setup will be connected to the GBTx ASIC. The internal controller implements a dedicated communication protocol.

Communication protocol
The GBTx ASIC [5] is developed at CERN and will be used in many experiments. However, in the CBM experiment it must be able to communicate with STS/MUCH-XYTE2 chip via AC-coupled links. That resulted in the need to develop a dedicated protocol. The resulting Hit and Control Transfer Synchronous Protocol (STS-HCTSP) [6] ensures transmission of commands from the Data Processing Boards (DPBs) [7] to the STS-XYTE2 chip (downlink direction), and bandwidth efficient transfer of measurement data from STS-XYTE2 chip to the DPB boards (uplink direction). The protocol uses the 8b/10b encoding to ensure correct transmission via AC coupled links. However, the GBTx uses a synchronous transmission with separate out-of-phase data lines (E-Link, with 180 Mbit uplink and 320 Mbit downlink). To compensate the skew between the clock and data lines, it is necessary to use the phase adjusted GBTx side clock and data lines (GBT-clock data). Therefore, special 2b/8b long sequences (EOS and SOS) distinguishable from 8b/10b encoded data, are used in the synchronization procedure to find the correct settings. The final solution uses central length frames (6-8 bytes after encoding in the downlink direction and 3 bytes, 30-30 bytes after encoding in the uplink direction). After proper synchronization on both sides, the data are transmitted at constant, deterministic, constant delay in the downlink direction. That allows using the link also during the reference clock and time to the front-end electronics.

Need for a tester
Due to the innovative design of the STS/MUCH-XYTE2, it is necessary to verify operation of its control part with the proposed communication protocol before ASIC tape-out. The tester will be part of the STS/MUCH-XYTE2 and the DPB board with the communication interface. As the hardware platform for the tester was chosen the AFCK board [8], that is also used as test platform prototype for the readout boards for the CBM readout chain [7]. To allow proper AC coupling of the differential links, a dedicated multichannel bi-directional FMC/HVIC adapter board was developed. It is possible to test different link technologies and cabling solutions by simple replacement of the FMC boards.

Implementation of the tester firmware

STSMUCH-XYTE2 model
Due to inherent differences between the FPGA and ASIC technologies, the HDL code [in System Verilog or Verilog] implementing the STS/MUCH-XYTE2 model for FPGA implementation. Special measures were applied to ensure coherency of FPGA and ASIC implementation. The following features had to be implemented differently in ASIC and FPGA model:
- Clocks driven by a frequency divider (in FPGA they have to be emulated with gated clocks).
- DDR outputs (in FPGA it is necessary to use the ODDR block).

Implementation of the STSMUCH-XYTE2 interface
That block (in short: STS-HCTSP Interface) implements the transmitter responsible for sending the downlink frames and receiver that receives the uplink frames. The uplink frames are then analyzed and then retransmitted to controller. That is essential, as the bit rate is designed to be high and the data are transmitted to the readout FIFO. The receiver is also equipped with separate decoders of special sequences (EFS and SOS) and selected synchronization characters (K improbable, 1,2,8,5), that are used for the link synchronization.

The STS Interface is also implemented in the model of the E-Link with adjustable delays on the clock out and the data inputs. Those features in the real E-Link are provided by the GBTx ASIC. In the tester they had to be emulated:
- The adjustable clock delay - using the DRP controlled PLL2 block
- The 8b/10b encoded data can be decoded using the IDP implementation. The STS Interface is controlled via the IPbus [9] block that uses the UDP protocol via 1 Gbit Ethernet to exchange high-level communication (e.g. test PC and the tester FPGA). IPbus is also used to receive the generated hit data from the readout FIFO.

Tester software
The software for control of the STS/MUCH-XYTE2 tester was written in Python, to enable fast prototyping and possibility of interactive work.

The developed software implements the object interface to IPbus-accessible registers and a class for writing and reading the STS/MUCH-XYTE2 registers.

Two link synchronization procedures are implemented – one for the “full synchronization”, assuming the existence of the two time delays between over-clocking and data lines are known; and the second one for the “fast synchronization” which reuses the information acquired during the “full synchronization”, allowing the user to easily select which type of synchronization should be performed. The test software also allows defining which uplink (from STS/MUCH-XYTE2 to DPB) links are operated and the functional checks for the connection to the GBTx tester. The synchronization procedure is able to ensure proper communication as long, as at least one uplink is working. The software also receives simulated hit data, and stores them in the file. The strings may be easily modified by the user.

Performed tests and results
The tests were performed both in the single-board configuration and in the two-boards configuration. The same firmware was used in both cases, however in the two-boards configuration only the STS/MUCH-XYTE2 model was used to test GBTx and only the STS/HCTSP interface was used in the 2nd board. Results obtained in both configurations were the same. The tests were performed at central transfer speed (180 Mbit uplink and 320 Mbit downlink). The tests included thorough testing of the link synchronization procedure. Both “full” and “standard” synchronization procedures were tested, and some problems related to the recovery from situations where the uplink links were incorrectly masked were identified. After necessary corrections both synchronization procedures and recovery from potential problems (e.g. masking of all communication links in the STS/MUCH-XYTE2 due to SEU or software error) were successfully tested. Results of successful tests were used to improve the protocol specification and related controller implementations.

Access to the STSMUCH-XYTE2 registers and reception of simulated hit data were also successfully tested.

Conclusions
The tests performed with the described system have proven correct operation of the digital part of the STS/MUCH-XYTE2 used with the developed communication protocol. Presented methodology allows testing of FEI ASIC before the real chip is available. The gained experience may be used to model ASIC specific features in FPGA. The STS/MUCH-XYTE2 interface core may be used to test also other FPGA systems using the GBTx-based E-Links. The whole solution will be further developed towards the test platform for the fabricated ASIC responses to be emulated E-Link. The firmware and software will also be the basis for development of components of the CBM readout chain.

Acknowledgment
Work was supported by GSI. The AGH work was supported by Polish Ministry of Science and Education.

References