Versatile ASIC and Protocol Tester for STS/MUCH-XYTER2 in CBM Experiment

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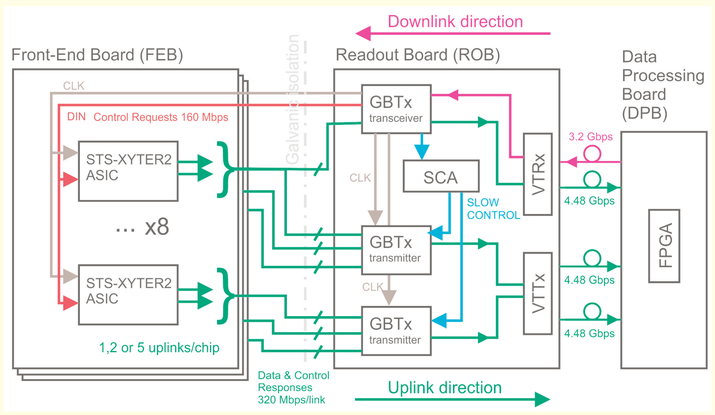
Introduction

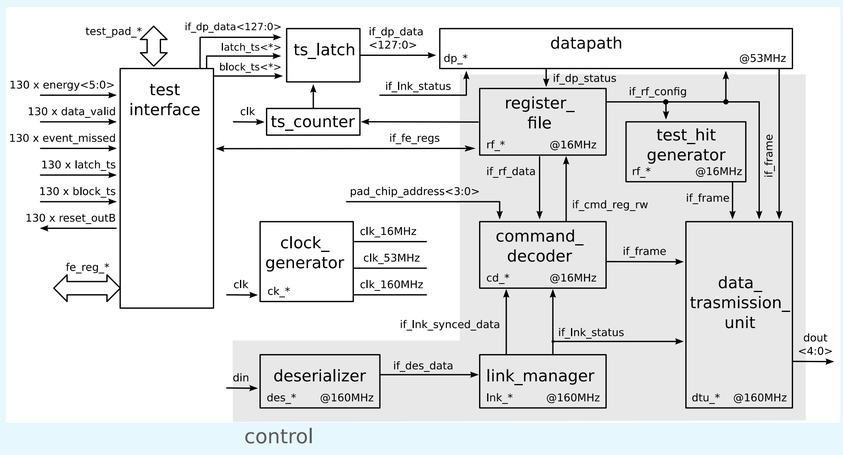
The Compressed Baryonic Matter (CBM) experiment is one of the experiments prepared at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt. Its main aim is the exploration of the QCD phase diagram in the region of high baryon densities during high-energy nucleus-nucleus collisions [1].
CBM will utilize various particle detectors: Micro Vertex Detector (MVD), Ring Imaging Cherenkov Detector (RICH), Transition Radiation Detector (TRD), Time of Flight Detector (TOF), Projectile Spectator Detector (PSD), Silicon Tracking System (STS), Muon Chamber (MUCH). The readout system for two of them - STS and MUCH will be based on the dedicated ASIC - STS/MUCH-XYTER2.



Proposal of the STS readout chain in the CBM experiment

STS/MUCH-XYTER2

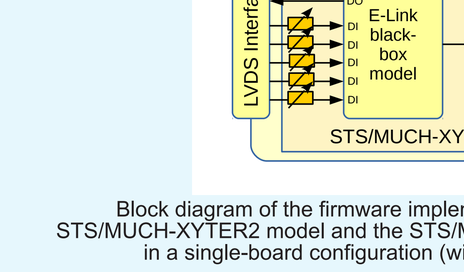
The STS/MUCH-XYTER2 [2] is an ASIC implemented in CMOS technology, which measures both the charge produced by the connected detector in 128 input channels (with 5-bit resolution) and the incident time. The STS/MUCH-XYTER2 offers also register files for the configuration of the chip and the analog front-end (AFE) [3, 4]. Transmission of the measurement data and configuration commands is provided by the serial multidrop communication interface using AC coupled SLVS lines, that in the final setup will be connected to the GBTx ASIC. The internal controller implements a dedicated communication protocol.



Simplified block diagram of the digital part of the STS/MUCH-XYTER2

Communication protocol

The GBTx ASIC [5] is developed at CERN and will be used in many experiments. However, in the CBM experiment it must be able to communicate with the STS/MUCH XYTER2 chip via AC-coupled links. That resulted in the need to develop a dedicated protocol. The resulting Hit and Control Transfer Synchronous Protocol (STS-HCTSP) [6] ensures transmission of commands from the Data Processing Boards (DPBs) [7] to the STS-XYTER2 chip (downlink direction), and bandwidth efficient transfer of measurement data from STS-XYTER2 chip to the DPB boards (uplink direction). The protocol uses the 8b/10b encoding to ensure correct transmission via AC coupled links. However, the GBTx uses a synchronous transmission with separate clock and data lines (E-Link, with 160 Mb/s uplink and 320 Mb/s downlink). To compensate the skew between the clock and data lines, it is necessary to use the phase adjusted GBTx clock and adjustable delays on GBTx data inputs. Therefore, special 20-bit long sequences (EOS and SOS) distinguishable from 8b/10b encoded data, are used in the synchronization procedure to find the correct settings. The final solution uses constant length frames (6-bytes, 60-bits after encoding in the downlink direction and 3 bytes, 30-bits after encoding in the uplink direction). After proper synchronization of the link, the protocol ensures constant, deterministic delay in the downlink direction. That allows using the link to distribute also the reference clock and time to the front-end electronics.

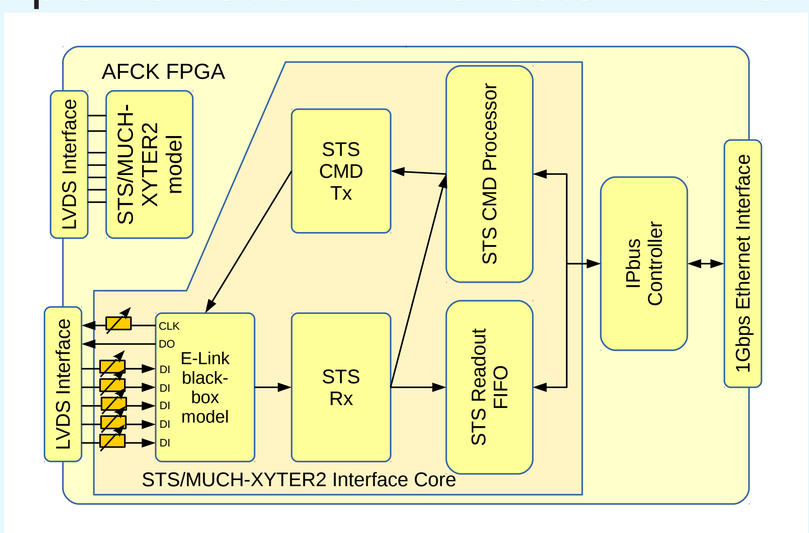


AFCK board with two connected FMC/VHDCI boards. The differential link is provided by the VHDCI cable.

Need for a tester

Due to the innovative design of the STS/MUCH-XYTER2, it is necessary to verify operation of its control part with the proposed communication protocol before ASIC tape-out. The tester must emulate the digital part of the STS/MUCH-XYTER2 and the DPB board with the communication interfaces.
As the hardware platform for the tester was chosen the AFCK board [8], that is also used as a prototype platform for the readout boards for the CBM readout chain [7].
To allow connection of long AC coupled differential links, a dedicated multichannel bidirectional FMC/VHDCI adapter board was developed. It is possible to test different link technologies and cabling solutions by simple replacement of the FMC boards.

Implementation of the tester firmware



Block diagram of the firmware implemented in the tester AFCK. The design implements both the STS/MUCH-XYTER2 model and the STS/MUCH-XYTER2 interface core. That allows performing tests either in a single-board configuration (with 2 FMC/VHDCI boards) or in two-boards configuration.

STS/MUCH-XYTER2 model

Due to inherent differences between the FPGA and ASIC technologies, the HDL code (in System Verilog) describing the STS/MUCH-XYTER2 design had to be adapted for FPGA implementation. Special measures were applied to ensure coherency of FPGA and ASIC implementations.
The following features had to be implemented differently in ASIC and FPGA model:

- Clocks driven by a frequency divider (in FPGA they had to be emulated with gated clocks).
- DDR outputs (in FPGA it is necessary to use the ODDR block)

Implementation of the STS/MUCH-XYTER2 interface

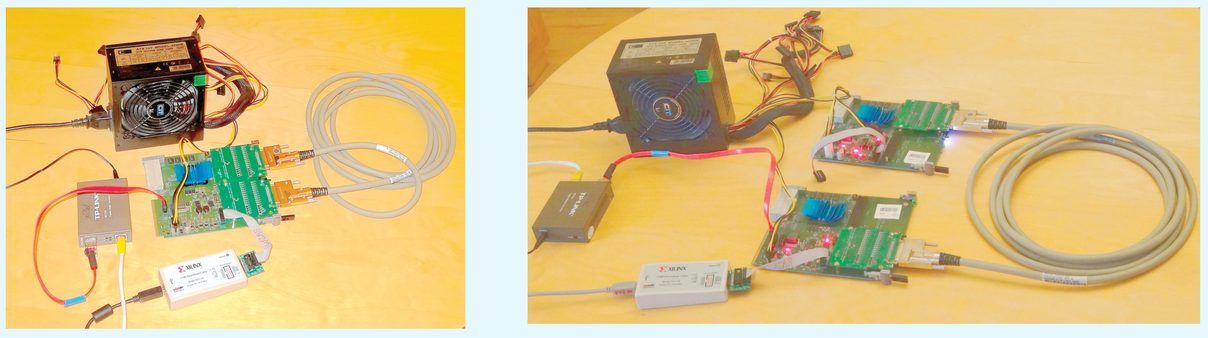
That block (in short: STS-HCTSP Interface) implements the transmitter responsible for sending the downlink frames and receiver that receives the uplink frames. The uplink frames are then analyzed and the responses to control commands are transferred to the command processor, while the hit data are transmitted to the readout FIFO. The receiver is also equipped with separate decoders of special sequences (EOS and SOS) and selected synchronization characters (K28.1, K28.5), that are used for the link synchronization.
The STS interface also includes the model of the E-Link with adjustable delays on the clock output and the data inputs. Those features in the real E-Link are provided by the GBTx ASIC. In the tester they had to be emulated:

- The adjustable clock delay - using the DRP controlled PLLE2 block
- The adjustable data delays - using the IDELAYE2 blocks

The STS Interface is controlled via the IPbus [9] block that uses the UDP protocol via 1 Gb/s Ethernet to provide bidirectional communication between the host PC and the tester FPGA. IPbus is also used to receive the generated hit data from the readout FIFO.

Tester software

The software for control of the STS/MUCH-XYTER2 tester was written in Python, to enable fast prototyping and possibility of interactive work.
The developed software implements the object interface to IPbus-accessible registers and a class for writing and reading the STS/MUCH-XYTER2 registers.
Two link synchronization procedures are implemented – one for the „full synchronization", assuming that no correct time/phase relations between outgoing data and clock, and incoming data are known; and the second one for the „fast synchronization" which reuses the information acquired during the „full synchronization". The user can easily select which type of synchronization should be performed. The test software also allows defining which uplink (from STS/MUCH-XYTER2 to DPB) links are operational. That functionality was used to test if the implemented synchronization procedure is able to ensure proper communication as long, as at least one uplink is working. The software also receives simulated hit data, and stores them in the file. The scripts may be easily modified by the user.



Test setups for single-board and two-boards configurations

Performed tests and results

The tests were performed both in the single-board configuration and in the two-boards configuration. The same firmware was used in both cases, however in the two-boards configuration only the STS/MUCH-XYTER2 model was used in the 1st board, and only the STS-HCTSP interface was used in the 2nd board. Results obtained in both configurations were the same. The tests were performed at nominal transfer speed (160 Mb/s uplink and 320 Mb/s downlink).
The tests included thorough testing of the link synchronization procedure. Both „full" and „standard" synchronization procedures were tested, and some problems related to the recovery from situations where the uplink links were incorrectly masked were identified. After necessary corrections both synchronization procedures and recovery from potentially disastrous situations (e.g. masking of all communication links in the STS/MUCH-XYTER2 due to SEU or software error) was successfully tested. Results of successive tests were used to improve the protocol specification and related controllers implementations.
Access to STS/MUCH-XYTER2 registers and reception of simulated hit data were also successfully tested.

Conclusions

The tests performed with the described system have proven correct operation of the digital part of the STS/MUCH-XYTER2 used with the developed communication protocol.
Presented methodology allows testing of FEE ASIC before the real chip is available. The gained experience may be used to model ASIC specific features in FPGA.
The STS/MUCH-XYTER2 interface core may be used to test also other FEE systems using the GBTx based E-Links. The whole solution will be further developed towards the test platform for the fabricated ASIC, both using the emulated E-Link and real GBTx. Both firmware and software will also be the basis for development of components of the CBM readout chain.

Acknowledgment

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