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Versatile ASIC and Protocol Tester for STS/MUCH-XYTER2 in CBM Experiment

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The STS/MUCH-XYTER2 is the new front-end ASIC for the STS and MUCH detectors in the CBM experiment. It uses an innovative protocol ensuring reliable synchronization of the communication link between the controller and the ASIC, transmission of time deterministic commands to the ASIC and efficient readout within a GBT-based data acquisition structure. The paper describes the FPGA-based tester platform for in-hardware functional verification of the digital part of the chip and the protocol before the ASIC is taped-out. The applied methodology may be useful for verification of other ASIC-based designs.

Summary

The STS/MUCH-XYTER is the new front-end ASIC designed for the STS and MUCH detectors in the CBM experiment. It uses an innovative protocol (STS-HCTSP) for sending the control commands to the ASIC in a time-deterministic way and for efficient reception of the hit-related data. An important feature of the protocol is that it enables a reliable synchronization and resynchronization of the communication link between the readout controller and the front-end ASIC without the full reset. That facilitates debugging of the readout system in case of problems.

The aim of the work was the development of a hardware platform for two purposes:

- the hardware verification of the ASIC control part before the tape-out
- the preparation of the basis for further development of the full readout system. Basing on these two goals, a dedicated hardware platform was prepared based on the AFCK board.

The presented methodology covers a number of specific issues both on the software and on the hardware level.

Due to inherent differences between the FPGA and ASIC technologies, the HDL code describing the STS/MUCH-XYTER2 design had to be adapted for FPGA implementation. Special measures were applied to ensure coherency of FPGA and ASIC implementations.

The dedicated controller module (communicating with the ASIC model under test) was also implemented as an IP core in FPGA. It implements time-critical parts of the communication protocol - transmits commands to the ASIC, handles responses and acknowledgments and receives the hit data.

The high-level procedures of the communication protocol, including the synchronization procedure and reception of data were implemented in a PC software using Python language. The communication between the computer and tester was provided by the Ethernet TCP/IP network with IPbus protocol. That approach allows rapid prototyping in Python prior to the C/C++ implementation of performance-critical parts after the algorithm is tested.

The communication link between the STS/MUCH-XYTER2 ASIC and its controller (AFCK-based boards) in the final system will be provided by the GBTx chip (featuring electrical links on the ASIC side and fast, optical link at the controller-side). As it was not available at the time tests were performed, the tester platform implements the realistic black-box model of the GBTx-based E-Link. The

tester platform also provides the AC-coupled differential links equivalent to the SLVS links which will be used in the final system.

The tests performed at the nominal speed of the STS/MUCH-XYTER2 links (160 Mbps uplink and 320 Mbps downlink) have proven the correctness of the ASIC's back-end model design and the communication protocol. The developed platform will be developed further towards a testplatform for the fabricated ASIC including the real GBT links. It can also be used as a prototype of the final ASIC controller implemented in the Data Processing Board.

The platform and associated methodology may be also reused in pre-production verification of other ASIC-based control and readout systems.

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