Contribution ID: **118** Type: **Poster**

HDI Flexible Front-End Hybrid Prototype for the PS Module of the CMS Tracker Upgrade

Tuesday 27 September 2016 17:24 (1 minute)

The CMS tracker upgrade for the HL-LHC relies on different module types, depending on the position of the respective module. They are built with HDI flexible circuits that are wire bonded to silicon strip sensors. The front-end hybrids will contain several flip-chip bonded readout ASICs that are still under development. Mock-up prototypes are used to qualify the advanced flexible circuit technology and the parameters of the hybrids. This paper presents the PS mock-up hybrid in terms of testing, interconnection, fold-over, thermal properties and layout feasibility. Plans for connectivity testing and simulation results are described.

Summary

A major upgrade of the CMS Tracker detector is today under development to address the new requirements imposed by the HL-LHC. The new CMS Tracker will use two main types of modules. The outer tracker 2S modules contain two parallel strip sensors of 10 × 10 cm2, enabling the identification of stubs required for the track triggering function. The inner tracker PS modules contain a strip sensor and a macro pixelated strip sensor of 5 × 10 cm2, providing additional track information along the Z-axis. The front-end electronics of these different modules are based on binary readout ASICs (CBC3, SSA, MPA), flip-chip bonded on different high density interconnection (HDI) flexible printed circuit boards.

The module development for the upgrade started well before the first ASIC prototypes were manufactured. One of the main module building blocks is the front-end hybrid. The first hybrid prototypes were designed for the 2S modules, using the CBC2 prototype. The first full scale front-end hybrid prototype was designed and manufactured in 2014. It enabled the construction of the first 2S module prototypes and it provided valuable feedback to the engineers. Several complications and difficulties were found and this highlighted how important it is to construct module prototypes in order to understand the arising problems.

The MPA, SSA and CIC ASICs of the PS front-end hybrid are still under development, however the corresponding module design is in a well-developed state. This required the design of a new PS type hybrid prototype in its targeted outline, which matches the current 3D design geometry of the module. It contains carbon fiber stiffeners that are glued on the bottom of the circuit to provide sufficient cooling and stiffness. Heating resistors and dummy chips are mounted to emulate the power consumption and mechanical behavior of the ASICs. The circuit also has a flexible fold over part that will bring useful information about the folding process.

Moreover, the PS mock-up prototype will be used for the electrical characterization of the powering, testing, data transfer and calibration features that are intended to be used in the final PS hybrids. It enables the evaluation of miniature power and interface connectors aimed to replace the initially foreseen wire bonded connections. Connectors could reduce the module assembly time and provide less fragile connection. Additionally, a fine pitch spring loaded needle tester pad pattern is implemented and evaluated: two probing patterns are used for contact resistance, cross talk, signal integrity, reliability and alignment tests. The folding impact on the differential impedance brings another subject for verification. Two different test options for the sensor connectivity with the front-end chips are implemented with known failures on the PCB level. One method is using antennae to inject charge into the wire bond pads. Second method is grounding the input channels of the chips and uses the internal charge injection of the front-end ASICs. This is necessary for the qualification of the hybrid connectivity during the production phase.

Primary author: KOVACS, Mark Istvan (CERN)

Co-authors: HONMA, Alan (CERN); BLANCHOT, Georges (CERN); BONNAUD, Julien (CERN); GADEK, Tomasz (CERN)

Presenter: KOVACS, Mark Istvan (CERN)

Session Classification: POSTER

Track Classification: Packaging