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System-Level Considerations of the Front-End Readout ASIC in the CBM Experiment from the Power Supply Perspective

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Paper presents the Silicon Tracking System low-voltage power system design starting from the power budget and noise spectrum requirements resulting from the front-end chip design (STS/MUCH-XYTER2). Power-supply rejection ratio simulation results, estimation on how the simulated and measured noise spectra of the voltage regulators would affect the front-end electronics, power budget and selection of feasible powering scheme in the experiment including aspects of area, power efficiency and radiation hardness will be presented.

Summary

New fixed target experiments using high intensity beams up to 10 AGeV from SIS100 synchrotron presently being constructed at FAIR/GSI center are under preparation. Most of the readout electronics and power supplies are expected to suffer very high flux of nuclear reaction products and have to be radiation hard up to 3 MRad and sustain up to 10ˆ14/cmˆ2 of 1 MeV neutron equivalent in their life time. Moreover, the minimum ionising particles under investigation leave very little signals in the sensors therefore very low noise level amplitude measurements are required by the front-end electronics for effective tracking. Sensor and interconnecting microcable capacitance and series resistance in conjunction with intrinsic noise of the charge sensitive amplifier are dominant noise sources in the system, however, single-ended architecture of the amplifiers used in the charge processing channels implicit potential problem with noise contribution from the power supply sources. Strict system-level constraints leave very little freedom in selecting power supply structure optimal with respect to: power efficiency, power density on modules and cooling capabilities, but also noise injection to the front-end via the power supply lines. Noise level simulations of front end ASIC´s (STS/MUCH-XYTER2) and measurements´ results of power supply and conditioning electronics (selected DC/DC converter and LDO regulators) will be presented together with power supply structure in the Silicon Tracking System.

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