An Advanced Power Analysis Methodology targeted to the Optimization of a Digital Pixel Readout Chip Design and its Critical Serial Powering System

Sara Marconi[1,2,3], Stella Orfanelli[1], Michael Karagounis[4], Jorgen Christiansen[1], Pisana Placidi[2,3], Tomasz Hemperek[5]

1. **CERN** – SWITZERLAND   2. **INFN** – Section of Perugia, ITALY   3. **DI** – University of Perugia, ITALY   4. **Fachhochschule Dortmund**, GERMANY   5. **SiLab** – Bonn, GERMANY

I. INTRODUCTION

The HL-LHC pixel detectors for the ATLAS and CMS experiments require significantly increased rate capability and low material budget to deliver the required physics performance. To meet these goals, a new pixel chip in 65 nm CMOS technology is being designed within the RD53 collaboration adopting low power design techniques and integrating an on-chip shunt regulator that allows for a serial powering scheme across the detector modules.
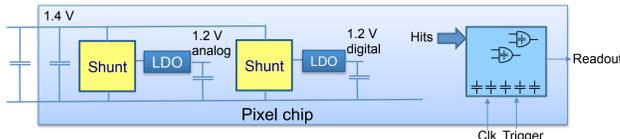
- For this scheme, a power supply per serial power chain will supply a constant current to the front-end chips. The I to V conversion will be done on-chip from two parallel powered shunt-LDO regulators [1], one for the analog and one for the digital domain. A shunt-LDO consists of:
  - a LDO regulator generating the low supply voltage
  - a shunt consuming the "surplus" current not drawn by the load
- A major worry is the presence of digital power variations, which could couple into the analog domain and if higher than the current provided to the serial chain, would cause chip failure.
- Considering averaging of power variations due to multiple stages of local decoupling and including a safety margin, the maximum current must be provided to the serial power chain.
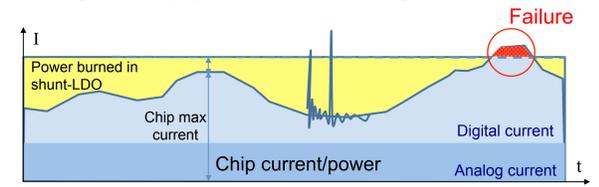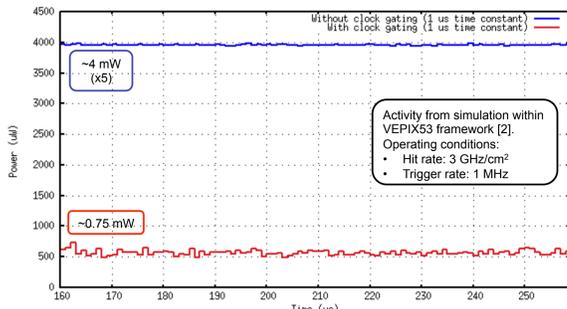
II. METHODOLOGY AND POWER RESULTS

a. Power estimation for architectural choices

One of the fundamental architectural choices to be made is related to the use of the clock gating technique :
- source of power variations;
- its use was initially discouraged to keep power more constant.

Power profiles from the gate-level description (64x4 array):
- significant increase in power consumption without any form of clock gating;
- more than x5 power increase to keep power constant can not be tolerated based on the chip specifications [3].

Activity from simulation within VEPIX53 framework [2]. Operating conditions:
- Hit rate: 3 GHz/cm^2
- Trigger rate: 1 MHz

~4 mW (x5)

~0.75 mW

b. Detailed power analysis after Place&Route

Need for post place-and-route power analysis:
- to early provide accurate specifications to the powering system;
- pure gate-level analysis shows around 50% underestimation (limited modeling of clock tree and parasitics).

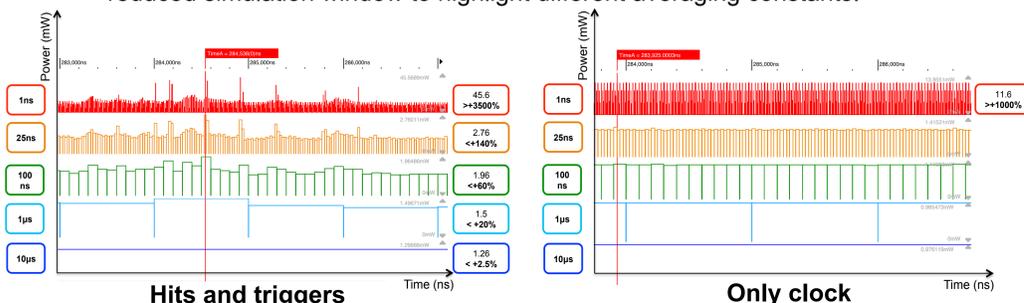**Average power estimations** under different corners and activity conditions.
- DUT: 64x4 pixel array with digital logic similar to the foreseen final chip;
- delay corner shown TYP (TYP RC corner, 25°C, lib: tcbn65lptc_ecsm, voltage 1.2);
- with fully extracted parasitics (.*spef* files).

Activity conditions	single pixel, digital	array 64x4	Final chip (400x400) digital
hits (3 GHz/cm^2) and triggers (1 MHz/cm^2)	4.84µW (52% clk tree)	1.24mW	0.774 W
only clock (~ -20%)	3.81µW (62% clk tree)	0.975mW	0.610 W
hits (3 GHz/cm^2) and no trigger(~ - 2.5%)	4.7µW (53% clk tree)	1.2mW	0.752 W

Analog power: ~ 5 µW/pixel

Dynamic power analysis achieved by extensive power profiling (i.e. look at power evolution over time):
- variety of operating conditions;
- peaks are evaluated at different time constants (1 ns, 25 ns, 100 ns, 1 µs, 10 µs);
  - short time constant (~ps-25 ns): should be filtered by on-chip decoupling
  - longer time constant (~1 µs): power averaged over such time window seen at the powering system level
- reduced simulation window to highlight different averaging constants.

1ns	45.6 >+3500%
25ns	2.76 <+140%
100 ns	1.96 <+60%
1µs	1.5 <+20%
10µs	1.26 < +2.5%

Hits and triggers

1ns	11.6 >+1000%
25ns	
100 ns	
1µs	
10µs	

Only clock

c. Application: optimization of pixel core logic

The power methodology is used for the optimization of the pixel array logic of the RD53 chip. A 8x8 hierarchical block (digital core), containing 2x2 pixel regions, is being optimized for power, area, hit efficiency (additional memory) and radiation tolerance;
- "peak power" is obtained with 1 µs averaging time constant.

8x8 digital core, hits and triggers activity TYPICAL corner	Average Power per pixel (µW)	Peak Power per pixel (µW)	Density
1. TOT counters, flip-flops for TOT storage, 7 mem, asynch read	4.8	6.26	89%
2. No TOT counter, latches for TOT storage, 7 mem, asynch read	5.6	6.54	85%
3. TOT counters, latches for TOT storage, 7 mem, asynch read	4.98	5.8	80%
4. TOT counters, latches for TOT storage, 7 mem, synch read	4.84	5.6	80%
5. TOT counters, latches for TOT storage, 8 mem, synch read	5.2	6.1	82%
same design as 5., but 500Mrad .lib for power analysis	5.39	6.06	same

Leakage is increasing ~x15, but still **not dominant**

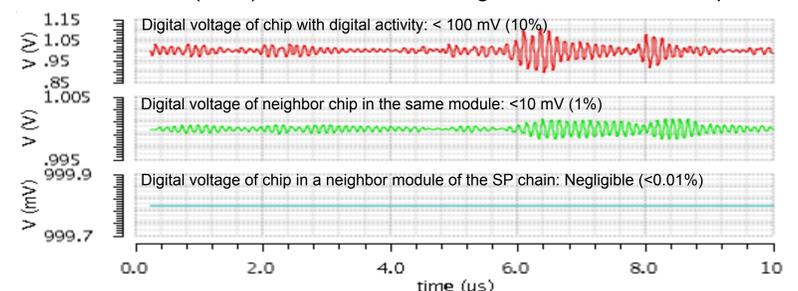## III. SHUNT-LDO SIMULATIONS WITH PROFILES

a. Topology and setup

- "Across-module serial power" is a current based powering scheme where modules are powered via constant current flowing from module to module and chips within a module are parallel powered.
- Two serially powered modules of four chips each were simulated based on the detailed shunt-LDO design.
- Local decoupling capacitances (chip's power grid, input/output shunt-LDO capacitors with ESR), parasitic inductances (wire-bonds, cabling), resistances and capacitances (pads) were also described.
- The digital activity of a chip was simulated as presented in the previous section (1 ns resolution) and the topology is shown in the sketch below.
- The impact of the digital activity to the rest of the serial power chain and the analog power domain of the chips was studied.
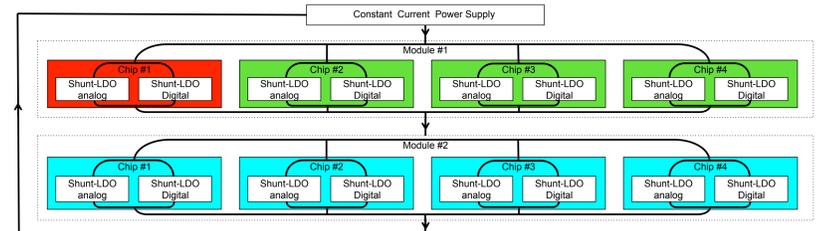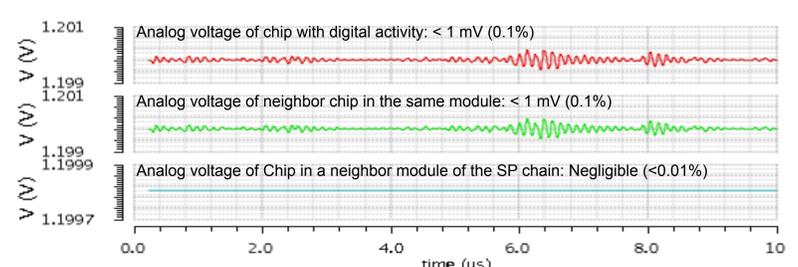
b. Impact of digital activity on digital voltage supply

- 100 mV variation (10%) is allowed for the digital domain of the chip.

Digital voltage of chip with digital activity: < 100 mV (10%)

Digital voltage of neighbor chip in the same module: <10 mV (1%)

Digital voltage of chip in a neighbor module of the SP chain: Negligible (<0.01%)

c. Impact of digital activity on analog voltage supply

- Only 10 mV variation (1%) is allowed for the sensitive analog part of the chip.

Analog voltage of chip with digital activity: < 1 mV (0.1%)

Analog voltage of neighbor chip in the same module: < 1 mV (0.1%)

Analog voltage of Chip in a neighbor module of the SP chain: Negligible (<0.01%)

IV. CONCLUSIONS AND FUTURE WORK

- The presented power analysis methodology has been successfully used for
  - architectural choices (e.g. clock gating)
  - detailed power profiling in realistic operation at different time constants
  - optimization of the critical digital array logic of the RD53 chip.
- The digital activity power profiles have been used as an input to a detailed system architecture of the serial powering topology, including the detailed shunt-LDO design and parasitics.
- The impact of digital power fluctuations to the digital and analog voltage supply of chips in the same or neighbor modules has been seen to be tolerable.
- Future steps include testing a prototype chip with the simulated shunt-LDO to confirm simulation results and new simulations under extreme conditions for power variations (background events, machine cycle, failure scenarios) for extensive verification.

References

[1] M. Karagounis et al., "An integrated Shunt-LDO regulator for serial powered systems," ESSCIRC 2009, Proceedings of, Athens, Greece, pp. 276-279.

[2] S. Marconi, E. Conti, P. Placidi, J. Christiansen and T. Hemperek, "The RD53 collaboration's SystemVerilog-UVM simulation framework and its general applicability to design of advanced pixel readout chips," Journal of Instrumentation, vol. 9, no. 10, p. P10005, 2014.

[3] M. Garcia-Sciveres, "RD53A Integrated Circuit Specifications". [Online]. Available: https://cds.cern.ch/record/2113263?ln=it, Dec 2015.