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An Advanced Power Analysis Methodology Targeted to the Optimization of a Digital Pixel Readout Chip Design and its Critical Serial Powering System

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A dedicated power analysis methodology, based on modern digital design tools and integrated with the VEPIX53 simulation framework developed within RD53 collaboration, is being used to guide vital choices for the design and optimization of the next generation ATLAS and CMS pixel chips and their critical serial powering circuit (Shunt-LDO). Power consumption is studied at different stages of the design flow under different operating conditions. Significant effort is put into extensively investigate dynamic power variations in relation with the decoupling seen by the powering network. Shunt-LDO simulations are also reported to prove the reliability at the system level.

Summary

New hybrid pixel detectors supporting hit rates up to 3GHz/cm2 and unprecedented radiation levels will be developed by the RD53 collaboration between ATLAS and CMS experiments at HL-LHC. In this scenario the design of complex digital logic at the lowest possible power consumption requires special techniques to develop a reliable system. This is dictated by the need for a serial powering scheme, required to overcome the insurmountable limits of a standard parallel powered mode for system modules featuring high granularity.
In this context, the baseline scheme features modules placed in series and powered by a constant current. The Shunt-LDO circuit, composed of a LDO regulator generating the low supply voltage and a shunt consuming the current not drawn by the load, will be used. Therefore, the constant current flowing in the serial power chain will be determined by the maximum current required by the chip, which should be minimized. These requirements demand a different approach with respect to well-established digital low power methodology. In this work a dedicated power analysis methodology, based on modern digital design tools and integrated with the VEPIX53 simulation framework developed within RD53 collaboration, is defined to guide vital choices for the design and optimization of both the chip and the Shunt-LDO.
The methodology presented is applied to a 65 nm pixel array, featuring similar characteristics to the foreseen RD53 pixel chip. Power behaviour is evaluated at different stages of the design flow, from early RTL/gate-level to detailed post P&R under different operating conditions. First, in order to drive architectural choices (e.g. critical use of clock gating) power estimations are performed at RTL/gate-level and power profiles are produced, thanks to the definition of an iterative algorithm. Simulations performed under RD53 operating conditions show a significant increase in power consumption when excluding any form of clock gating in the architecture, less tolerable than the power variations caused by it. Second, more detailed power analysis (post P&R) is necessary to provide accurate specifications to the powering system, whereas gate-level analysis shows around 50% underestimation. Average power estimations are obtained under different corners and activity conditions (e.g. extreme hit and trigger rate, consecutive triggers, high hit rate and trigger absence, just clocking the logic), in order to assess power impact of different factors, important to understand variations in different operation modes and guide design choices. Power variations, particularly critical for the target system, are also studied with extensive power profiling under the variety of operating conditions. Moreover, since low-pass filtering will be seen from the chip to the serial power network (due to on-chip decoupling, shunt-LDO decoupling, module decoupling), power peaks are evaluated at different time constants

(1ns, 25ns, 100ns, 1 µs, 10 µs) and qualified on-chip decoupling estimation is performed to identify the critical time constant. Power profiles are also used as an input to Shunt-LDO simulations to verify its functionality and demonstrate the reliability of the powering scheme.

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