# Testing of hybrid circuits for the CMS Tracker Upgrade of front-end electronics

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## Abstract

*The upgrade of the CMS tracker for the HL-LHC requires the design of new double-sensor, front-end modules, which implement L1 trigger functionality in the increased luminosity environment. Each of these new modules will contain two different, high density front-end hybrid circuits, equipped with flip-chip ASICs, auxiliary electronic components and mechanical structures. The hybrids have to be functionally tested, before they are assembled into modules. Test methods are proposed together with their corresponding testing hardware and software. They feature functional tests and signal injection in cold environment aiming at finding the possible failures of the hybrids under real operating conditions.*

## Introduction

Current plans for the future CMS Tracker layout assume the use of more than 14,000 tracking modules. In total over 28,000 front-end hybrids of ten different variations will be produced. To ensure a high yield of fully functioning modules, the hybrids must be tested before they are used for the assembly. Testing should allow tracking of all possible failures affecting hybrids performance.

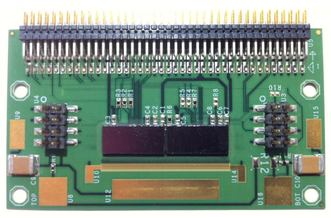

*Figure: A photo of the 2CBC2 hybrid*

To achieve these goals, the testability of stand-alone hybrids became an important factor. This brings several constraints on the circuits and front-end ASICs designs. One should try to: include control features within the ASICs, provide a functionality of front-end channels internal stimulation, add a quick way of interfacing the hybrid and implement test features directly in the PCB. These properties simplify thorough testing of sensorless hybrid circuits prior to the module assembly.

Proposed testing procedures were created based on functionalities implemented in the CMS Binary Chip (*CBC2*). Two platforms hosting the mentioned chip, shown in the photos, were used during the development stage. Another hybrid being produced (later referred to as *PS prototype hybrid*) contains known failures and will be used as a validation platform. Details in the poster: *'HDI flexible front-end hybrid prototype for the PS module of the CMS tracker upgrade'* by M. Kovacs et al.

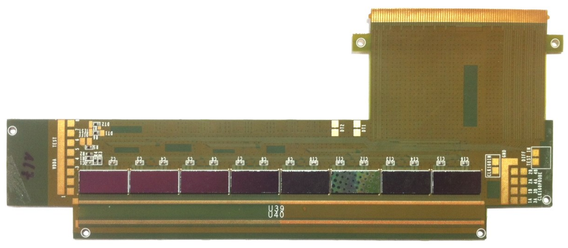

*Figure: A photo of the 8CBC2 front-end hybrid*

## Testing scheme and setup

Functional tests foreseen for the hybrid qualification consist of:

- electric current consumption monitoring,
- validation of ASICs configurability by performing write and read operations on their registers,
- input channels testing, which includes:
  - a full calibration of all input channels present in the hybrid,
  - a test of wire bond pads to ASIC connectivity,
  - a diagnosis of channels mutual interconnection performed to detect shorts between them.

The testing routine will be performed at room and low temperature by cooling the hybrids directly via their thermal contacts. The low temperature testing is intended to be representative of the tracker operating conditions. A setup was designed to keep the tested hybrid in a controlled dry air environment while cooling it with two Peltier modules.

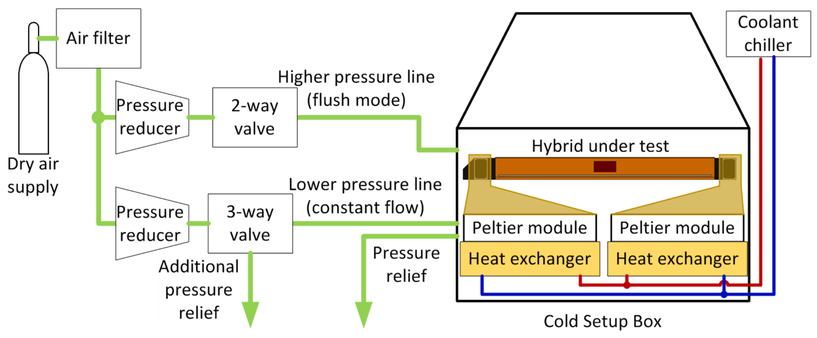


*Figure: Schematics of the dry air injection and cooling systems for hybrids cold testing*

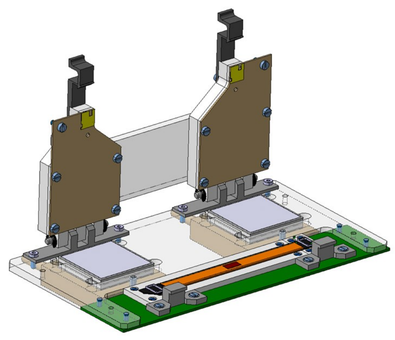

*Figure: 3D design of the cold test setup (this device is placed inside the test box)*

## Connectivity test of the ASIC input channels to wire bond pads

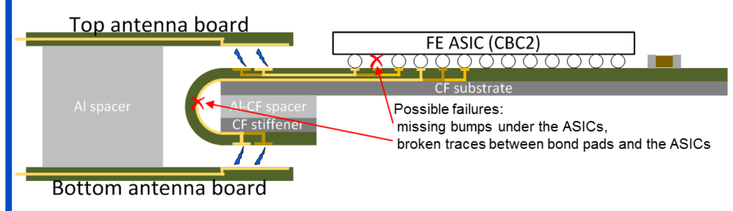


*Figure: A sketch of signal injection into folded 8CBC2 hybrid*

This method is meant to detect any discontinuity in the input signal paths of the hybrid, for example: missing bumps under the ASIC or broken traces. During this test a signal is capacitively coupled into the hybrid wire bond pads through two antenna boards.

Response of input channels is measured in the form of occupancy histograms. The testing algorithm looks for channels which show marginal activity in that process. These are either non-functioning or disconnected from the wire bond pads.

An early implementation of this method has uncovered a weakness in the response of the CBC2 to simultaneous stimulation of many channels, which will be corrected in the next version of the chip. To continue working with CBC2 in stable conditions the antenna strip was divided into small pads, which stimulate less than 30 input channels at a time. This new segmented antenna board is controllable from a PC via the USB interface. Another possibility of implementation of this method is a direct integration of the antenna in the hybrid. PS prototype hybrid will host this feature.

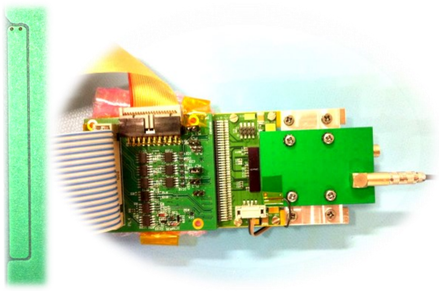

*Figure: Picture of a setup with two single-strip antenna boards for 2CBC2 hybrid testing*

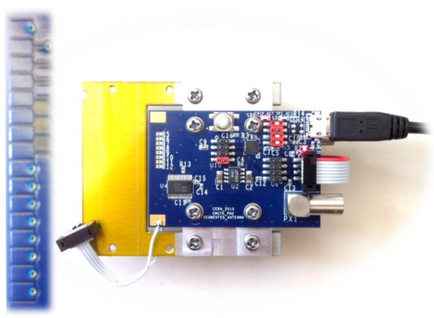

*Figure: Picture of a setup with two segmented antenna boards for 2CBC2 hybrid testing*

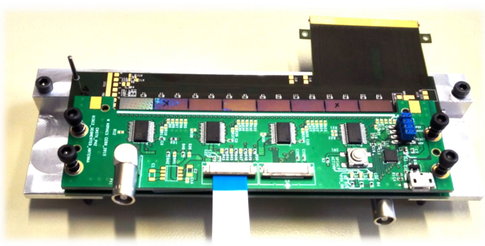

*Figure: Picture of a setup with two segmented antenna boards for 8CBC2 hybrid testing*

### Example A

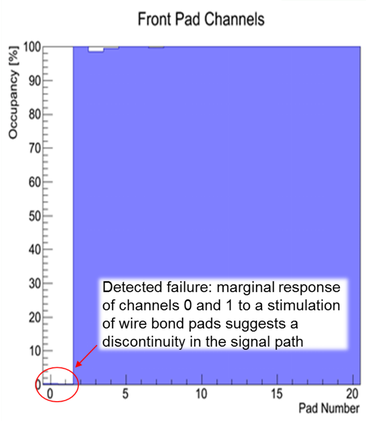


*Figure: Front channels histogram obtained during 2CBC2 antenna test*

The figure on the left hand side was an output of a segmented antenna test done on the 2CBC2 hybrid. It shows occupancy histograms zoomed at 21 front channels. Channels 0 and 1 show marginal activity while the signal is being injected to the wire bond pads. This suggests that the mentioned channels might be disconnected from their corresponding pads on the hybrid.

## Detection of mutual interconnections between FE ASIC input channels

This method is meant to detect shorts between input channels, which due to the fine pitch of traces and use of the flip-chip technology cannot be visually inspected. Inner test pulse generator is used as a signal source in this case. If two channels are shorted, while injecting a pulse into one of them, the other one will show similar activity thus can be identified by the algorithm. This method has been validated on many hybrids with very accurate results.

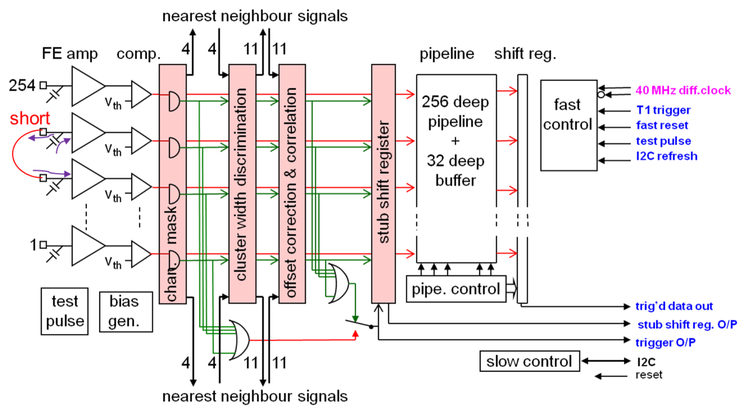


*Figure: CBC2 signal path with shorted channels 253 and 252*

Most common failures appearing in the assembled 8CBC2 hybrids are shorts between bumps under the ASICs. The main concern are shorts between input channels as they directly affect tracking quality of the module and are difficult to spot. Other shorts than these ones are easier to detect. A short between data lines results in a non-sense read out, whereas a short between power lines causes extensive current drain.

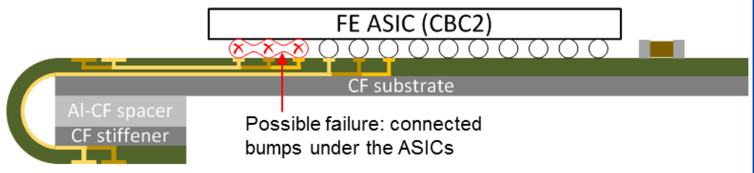


*Figure: A cross-section sketch of a folded 8CBC2 hybrid with shorted bumps*

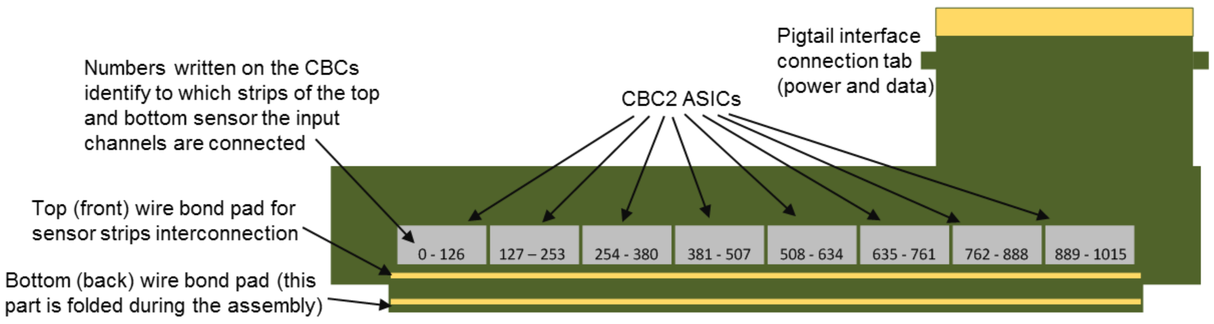


*Figure: An explanatory sketch of an unfolded 8CBC2 hybrid components*

### Example B

Outcome of the algorithm run on an 8CBC2 hybrid:

```
Shorted channels searching procedure
Sides: Front - 0  Back - 1 (Channel numbering starts from 0)

 Side   | Channel_ID   | Group_ID     | Shorted_With_Group_ID
-------------------------------------------------------------
   0    |       886    |       4      |       1
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
   0    |       883    |       1      |       4
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
```

Detected shorted channels are both belonging to the seventh CBC2 mounted on this hybrid.

X-ray image of mentioned chip revealed the source of the short, which in this case was an interconnection between bumps of input channels under the ASIC.

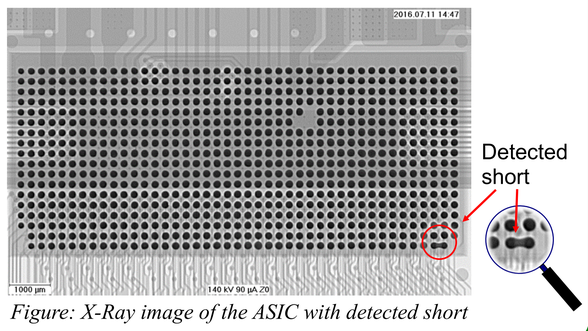


*Figure: X-Ray image of the ASIC with detected short*

The described procedure can also be applied during the assembly of the modules. After wire-bonding of the sensors to the hybrids one may use it to find shorts between wire-bonds or among the wire bond pads. Detected shorts can be fixed before the encapsulation of wire-bonds thus improving the quality of modules.

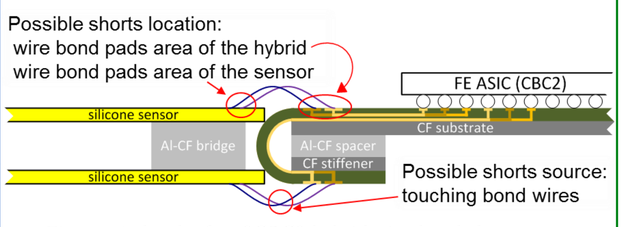


*Figure: A sketch of an 8CBC2 hybrid wire-bonded to sensors*

The algorithm has proven its effectiveness during numerous hybrid tests. Moreover, it was run on a prototype module where it revealed a very small short caused by a scratch on the sensor wire bond pads. This type of short would be hard to discover by a visual inspection.

### Example C

Outcome of the algorithm run on a module:

```
Shorted channels searching procedure
Sides: Front - 0  Back - 1 (Channel numbering starts from 0)

 Side   | Channel_ID   | Group_ID     | Shorted_With_Group_ID
-------------------------------------------------------------
-------------------------------------------------------------
   1    |      1012    |       3      |       2
-------------------------------------------------------------
   1    |      1011    |       2      |       3
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
-------------------------------------------------------------
```

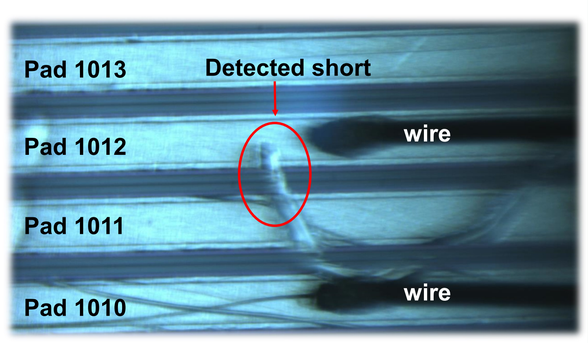


*Figure: A microscope image of the short between pads on the silicon sensor detected by the algorithm*

## Future development

There is one more test foreseen during hybrid testing routine. It involves the measurement of voltage drop along the hybrid meant to verify the quality of powering of mounted ASICs. Next steps of the development assume automatization of the testing setup and further verification of proposed testing methods. As a final step a common database needs to be created which is supposed to hold all of the testing results of each produced circuit.

## Conclusions

This study was conducted with a view to the development of a common protocol for hybrid circuits testing. The presented scheme and methods are meant to be used during the prototyping and production phase of the front-end electronics for the CMS Tracker upgrade. Principles of operation of proposed test methods are well defined and already implemented. The algorithms together with the corresponding hardware still have to be fully evaluated. In parallel to that, a cold testing setup is being developed which aims at re-creating temperature conditions of the new CMS Tracker.