## **TWEPP 2016 - Topical Workshop on Electronics for Particle Physics**



Contribution ID: 89

Type: Poster

## Testing of Hybrid Circuits for the CMS Tracker Upgrade of Front-End Electronics

Wednesday 28 September 2016 17:21 (1 minute)

The upgrade of the CMS tracker for the HL-LHC requires the design of new double-sensor, front-end modules, which implement L1 trigger functionality in the increased luminosity environment. These new modules will contain two different, high density front-end hybrid circuits, equipped with flip-chip ASICs, auxiliary electronic components and mechanical structures. The hybrids require qualification tests, before they are assembled into modules. Test methods are proposed together with their corresponding testing hardware and software. They feature functional tests and signal injection in cold environment aiming at finding the possible failures of the hybrids under real operating conditions.

## **Summary**

The future HL-LHC is imposing demanding requirements on its particle detectors. The luminosity increase results in higher radiation and data rate. A major upgrade of the CMS Tracker is foreseen to cope with these new constraints. It is designed to provide the most useful and accurate information about the trajectories of the collision products. To achieve these goals several features are implemented at the level of front end modules, such as lower mass, Level 1 track triggering functionality and a higher density of channels.

The future tracker structure is made of different versions of double-sensor modules that vary in the distance between their sensor planes and the type of sensors. Each module contains two high density front-end hybrid circuits. These hybrids host binary readout ASICs which are connected with strip sensors. Additionally, each hybrid is equipped with auxiliary electronic components and mechanical reinforcement structures, which also serve as a cooling interface. In total ten different hybrid geometries are foreseen in the design of the future tracker. It is planned to produce as many as thirty thousand pieces.

The hybrids need to be tested before they are used for module assembly. This step is crucial to ensure a high yield of fully functioning modules. The testing should allow tracking all possible failures affecting hybrid performance. The hybrid tests will be performed at room and low temperature by cooling hybrids directly via their thermal contacts. The low temperature testing is intended to be representative of the tracker operating conditions, requiring a specifically designed testing infrastructure with a humidity condensation protection feature.

The hybrid test parameters cover: the power consumption of the hybrid, the ASICs control registers accessibility, the functionality of input channels and fast data output interfaces. The input channels are connected with fine tracks to the bump bond pads on the front-end chips which cannot be visually inspected. The continuity must be specifically verified by other means. Developing a fast and reliable method for checking connectivity and functionality of all these channels has become a priority. The continuity checking techniques have been initially verified on prototype circuits based on CMS Binary Chip 2 (CBC2). Several testing methods have been investigated for ease of implementation, repeatability and accuracy. One method which has been extensively investigated is a contactless charge injection system. Early implementations of this method have demonstrated its effectiveness, and have uncovered a weakness in the response of the CBC2 to simultaneous stimulation of many channels, which will be corrected in the next version of the chip.

The performance results of the proposed testing methods are presented from the point of view of accuracy, difficulties of physical implementation and duration of the test process. This study was conducted with a view to the development of a common protocol for hybrid circuits testing.

Primary author: GADEK, Tomasz (CERN)

**Co-authors:** HONMA, Alan (CERN); RAYMOND, David Mark (Imperial College Sci., Tech. & Med. (GB)); BLAN-CHOT, Georges (CERN); KOVACS, Mark Istvan (CERN); ROSE, Pierre (University of Wisconsin-Madison (US))

**Presenter:** GADEK, Tomasz (CERN)

Session Classification: POSTER

Track Classification: Production