Test Strategies for Industrial Testers for Converter Controls Equipment

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Industrial Test Equipment Project

Power converters and their controls electronics are key elements for the operation of the CERN accelerator complex, having a direct impact on its availability. To achieve a high MTBF (Mean-Time-Between-Failure) and ways to verify equipment, a set of industrial testers is used for the electronics. The roles of the testers are to validate mass production during the manufacturing phase and to provide means to diagnose and repair failed modules that are brought back from the operation. Two main test system platforms were adopted: a PXI platform for mixed analogue-digital functional tests and a JTAG-BS (JTAG Boundary-Scan) platform for digital interconnection and functional tests.The paper is a follow-up after a similar paper at TWEPP2015 conference, including more test platforms (Boundary-Scan), and the outcome after test phase in production. We report on the test software and hardware design resulted in maximizing the test coverage and minimizing the test design effort.

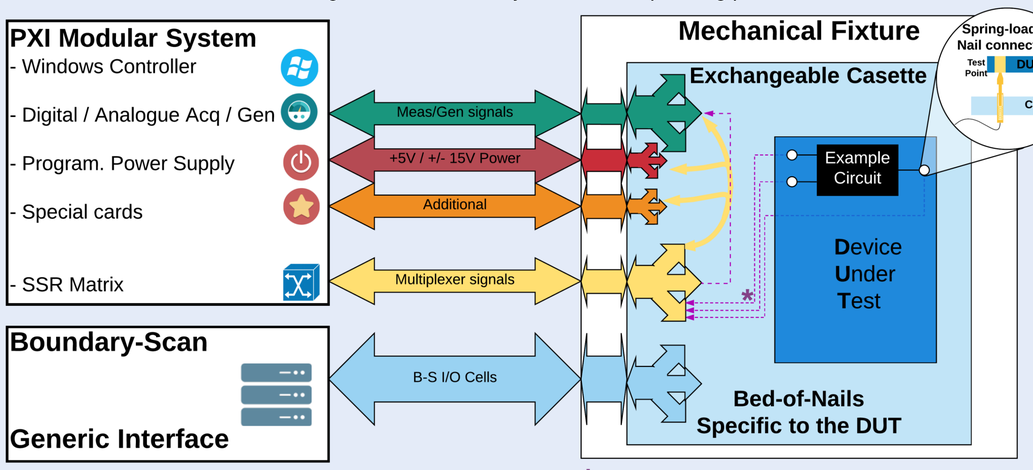
Unified Test Environment

Test equipment consists of 3 main parts: **PXI modular system** - a control PC and data acquisition and generation modular system, **Boundary-Scan Interface** - a generic digital I/O cell interface controlled by the PXI, separate software and hardware. The test interfaces of each of the platforms**(PXI and Boundary Scan**) are **connected** to a **mechanical fixture**. Then the **cassette** is interfacing them mechanically to the corresponding points on the DUT.

The measurement and generation functionalities of the PXI platform

- 3 channel Programmable PSU:
  - ❑ 0-6V @ 0-1A
  - ❑ 0-20V @ 0-0.5A
  - ❑ -20-0V @ 0-0.5A
- 32 analog inputs 16-Bit @ 250 kS/s
- 4 analog outputs 833 kS/s
- 236 digital I/O
- WorldFIP communication
- **SSR crosspoint matrix**
  - ❖ software-defined 4x64 relay matrix
  - ❖ can interconnect during the test execution
  - ❖ multiplexing analog and digital channels
  - ❖ the connection between the DAQ and matrix is done outside the PXI platform, in the exchangeable cassette which is specific to each DUT.
  - ❖ for each and every DUT the signals multiplexed by the card can be defined separately and the card is connected only to the fixture backplane.

PXI Platform



Roles of Mechanical Fixture

- Access test points and connectors of a DUT
- Reduce connection uncertainty
- Increase reliability and longevity

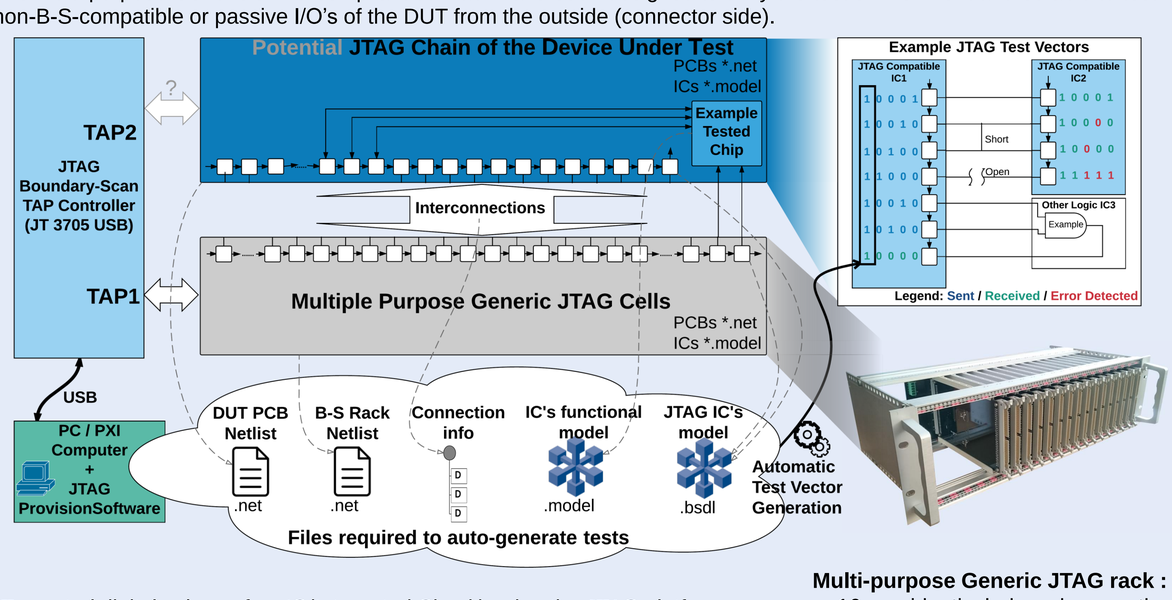
Mechanical Fixture

A modular construction (cassette) allows to easily exchange a module to fit a different DUT while maintaining all the test infrastructure connected to it.

JTAG Boundary-Scan

Most of the modern digital integrated circuits, especially programmable digital logic, is compliant with an **IEEE 1149.1** standard established by **JTAG**(Joint Test Action Group). The standard explains a relatively easy way to access most digital I/O cells of the integrated circuit with a 5 wire interface, that control a logic similar to a shift register.

The Multi-purpose Generic JTAG-compliant cell rack have been designed to unify the test environment and be able to test non-B-S-compatible or passive I/O's of the DUT from the outside (connector side).



To control digital values of an IC(Integrated Circuit) using the JTAG platform:

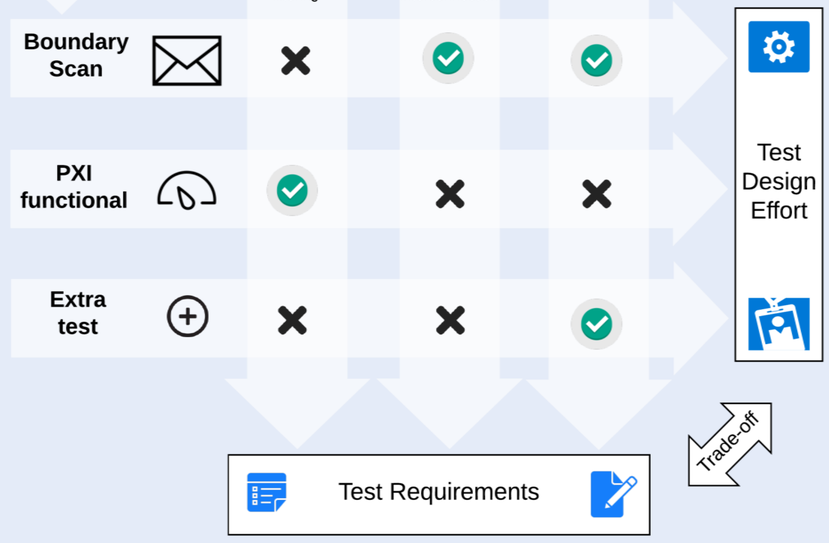
- It needs to be connected to a **JTAG chain**.
- The chain is managed by a **JTAG controller** through **TAP(Test Access Port).** The controller(JT 3705) used in the system has 2 TAPs, TAP 1 for the Multi-purpose JTAG Test Rack,TAP 2 for a JTAG chain of a DUT(if existing).
- **Tests vectors** are managed by the **test generation software** (JTAG Provision).
- The **test vectors** are **typically generated automatically** on the basis of the netlists, board-to-board interconnections and model files.

Multi-purpose Generic JTAG rack :

- 16 x identical boards on the passive motherboard
- Up to 1024 JTAG I/O cells in one chain
- Possibility to shorten the chain
- 3.3V output
- 2.4 - 5.5V input

Test Strategy

- **Test requirements** defined by **the design team** (**trade-off** with test design effort)
- **Test specification document** prepared and approved by the **design and the test teams** to understand problems and testability tradeoffs.
- **Test strategy** defined by the **test team** is **specific to each board**
- **Test strategy** depends on the **test design effort** and **needed test coverage**



Test Execution Plan

- **Tests are performed at CERN** to reduce risks associated with sending the test equipment on the site and technician's work assessment and validation.
- **Test report is generated automatically after test**. When all tests are finished, reports are collected into the database.
- **If all tests for the DUT are passed**, the ID and Barcode of the tested DUT are associated and added to the database of section equipment.
- **If any test is failed**, the boards are diagnosed and repaired.
- **Repetitive failures** are **reported to the manufacturer.**

Test Results - FGClite Testers

After each board is designed and a prototype functionally is validated, the process of production of boards can be described in the following steps:
1. component purchase,
2. PCB production (subcontractor 1),
3. assembly of boards (subcontractor 2),
4. unit tests at the reception at CERN.

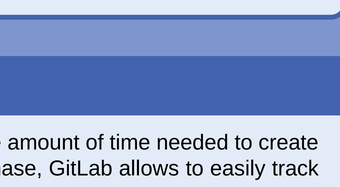
All failure data in this section is divided into two main groups:
1. Tester equipment failures not impacting the production but allowing the test team to improve on the test design
2. Production failures that will be analysed on case-by-case basis and will be communicated to the subcontractor.
The second group **2** contains three different classes of failures:
2a soldering failure,
2b component placement failure,
2c component failure.

Table with test results of FGCLite boards.

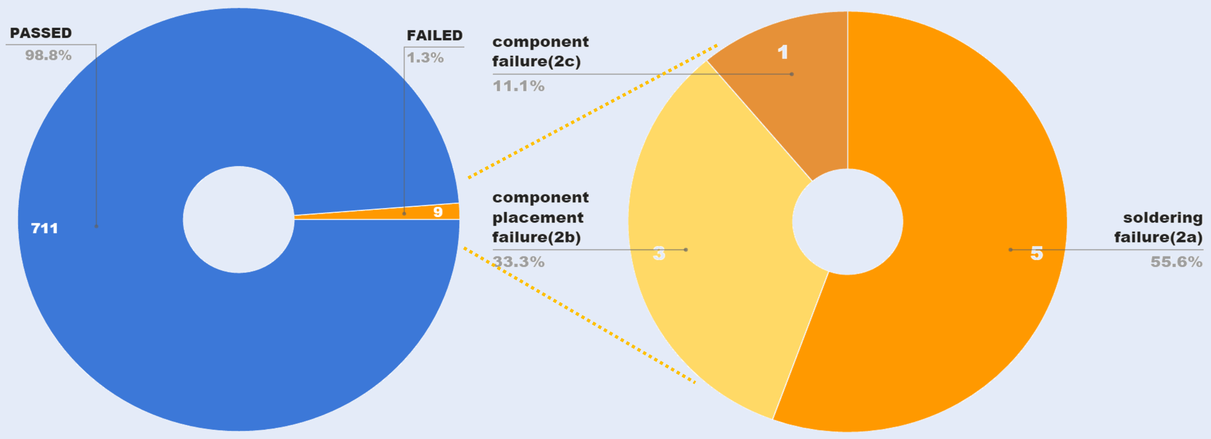
Board name	# Components	# Boards	# Failed boards	#Failed test.	Comments
FGClite MB	14	120	1	0	2b: Connector inversed
FGCLite CB	211	120	0	8	1: FPGA programming
FGCLite AB	298	120	5	0	2a: Pin of the relay not soldered 2b: Transistor absent 2a: DAC chip not correctly soldered 2a: Resistor network- Dry joint 2c: Resistor network - resistor open
FGCLite PB	112	120	0	1	1: 3V3 test point out of margin
FGCLite XB	111	120	0	0	
FGCLite IOB	249	120	3	0	2b: transistor absent 2a: pin of the relay not soldered 2a: pin of the transistor not soldered

Each individual board is tested with a dedicated PXI-based or Boundary-Scan tester. The boards from the subcontractor 2 are delivered in batches of several tens to several hundreds and before each subsequent batch is being assembled, CERN feeds back the failure statistics to the subcontractor 2, giving either the green light to continue the assembly process or working with the subcontractor 2 to improve on their assembly process to meet CERN's yield requirements.

The only PXI tester problems(noted with **1** in the comment section) were related to a requested value margin and automated programmation of the 2 FPGA's present on the FGCLite CB board. After the first phase of using the testers, the failures were gathered and tests were changed within a short time period. It was possible because both PXI-based and Boundary-Scan platforms are executed within the test software that is easy to change and recompile during the first test-phase.



Example soldering failure(2a) of the DUT (FGClite AB)



Conclusions

By using multiple design platforms and fitting the test strategy accordingly, it is possible to test very complicated boards with the relatively small design effort and manpower. Thanks to the B-S automated test generation, the amount of time needed to create a test platform(test development efficiency) has decreased dramatically in the section. For these tests the test design itself is often almost removed from test design workflow. During unit test development and validation phase, GitLab allows to easily track changes, effort and organizes the development process In the presented test strategy the balance between DUT coverage and test development time is maintained and also agreed with the group of DUT designers.

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