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Single Event Effects Mitigation with TMRG Tool

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Single Event Effects (SEE) are a major concern for integrated circuits exposed to radiation. There have been several techniques proposed in order to protect the circuits against radiation induced upsets (e.g. Triple Modular Redundancy). The purpose of the TMRG tool is to automatize the process of triplicating digital circuits freeing the designer from introducing manually the TMR code at the implementation stage. It helps to ensure that triplicated logic is maintained through the design process. Finally, the tool streamlines the process of introducing SEU and SET in gate level simulations for final verification.

Summary

Single Event Upsets (SEU) are a major concern for integrated circuits used in radiation environment, especially for circuits fabricated in modern deep sub-micron technologies. For reliable system operation in environments such as the LHC it is necessary to protect the logic from radiation induced Single Event Upsets (SEU). Many techniques have been proposed in order to protect the circuit against SEU. Virtually all techniques rely on data redundancy. It is assumed that if the information is stored in several places (circuit nodes), it can be properly reconstructed even if some of these nodes are disturbed. Among the SEU hardening techniques, some are based on hardening standard cells while others address the problem on a system level, by utilizing error-correcting coding (ECC), temporal redundancy, or Triple Module Redundancy (TMR).

The Triple Module Redundancy Generator (TMRG) tool developed at CERN automatizes the process of triplicating digital circuits freeing the designer from introducing the TMR code at the implementation stage. As the triplication does come with penalties (increased power and area, decreased speed) it is not always possible to fully triplicate the circuitry. Moreover, not all blocks can be easily triplicated (e.g. I/O ports or some analog blocks). The TMRG tool allows the designer to decide which blocks and signals should be triplicated. The tool handles the conversion process between triplicated and not-triplicated signals. The behavior of the tool is controlled by directives, which can be placed in the Verilog source code or a configuration file. The TMRG tool chain is compatible with the ASIC design flow used in the HEP community and does not over restrict the user's coding style. In addition, as it can be run in a batch mode, the tool can be seamlessly integrated in a fully automatic digital design flow.

The code generated by TMRG tool will contain redundancy and therefore the synthesizer will want to remove it, compromising the production of SEU/SET robust digital circuits. The TMRG tool chain helps to ensure that triplicated logic is maintained during the synthesis process by generating a set of constrains for the synthesis process. In modern deep sub-micron technologies, the probability of multiple bits upsets caused by the same particle is not negligible. In order not to compromise TMR effort, the redundant cells have to

be placed away from each other. Therefore, the TMRG tool chain assist also in the place and route, trying to constrain the placement process. Finally, the tool provides an uniform mechanism to introduce SEU and SET in gate level simulations for final verification.

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