Radiation Hardened by Design, Low Jitter, 2.56 Gbps LVDS/SLVS based Receiver in 65 nm CMOS

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Introduction

High precision time-domain signal processing circuits like CMS/ATLAS at CERN or laser-ranging sensors, contain information in the timing difference between multiple signals or events. In complex systems the distance between the detector and TDC can be rather large, calling for an accurate and long distance transmission of signals, here done by using LVDS/SLVS signals.

Because the LVDS/SLVS receiver is positioned in the signal path, any introduced timing distortion will cause a measurement error. Consequently, the jitter of the system must be minimized. Secondly, to allow an accurate measurement between multiple events, the propagation delay of all edges must remain the same.
This receiver introduces a replica with feedback loop which uses a 50 % duty cycle input clock to equalizes the propagation delays of the rising and falling edges and compensates for the variations introduced by PVT and radiation effects.

Schematic

- RX1: Accurate timing information
  - Equal propagation delay by balancing M6-M9
- RX2: Replica receiver
  - Compensates PVT and radiation effects.

When $T_{rise} = T_{fall}$:

Input: 50 % duty cycle

→ Output 50 % duty cycle

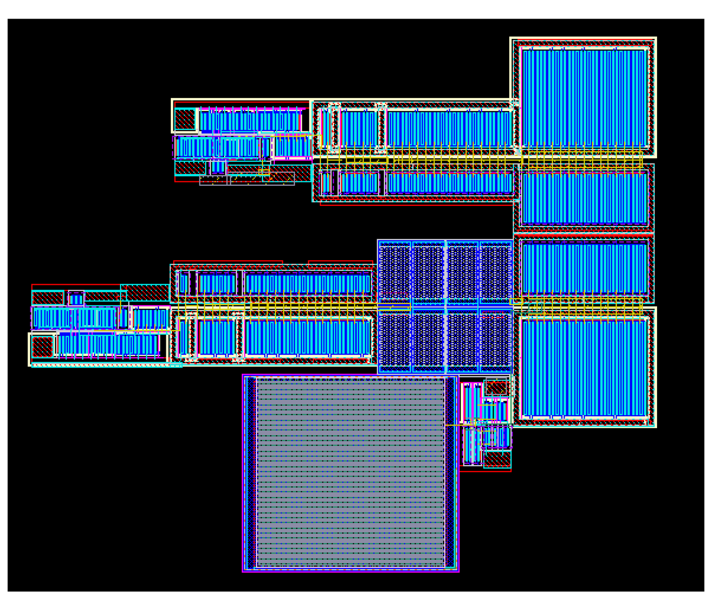
CP: IUP = IDOWN → V_{FB} = VDD/2

Propagation delay asymmetry = duty cycle error

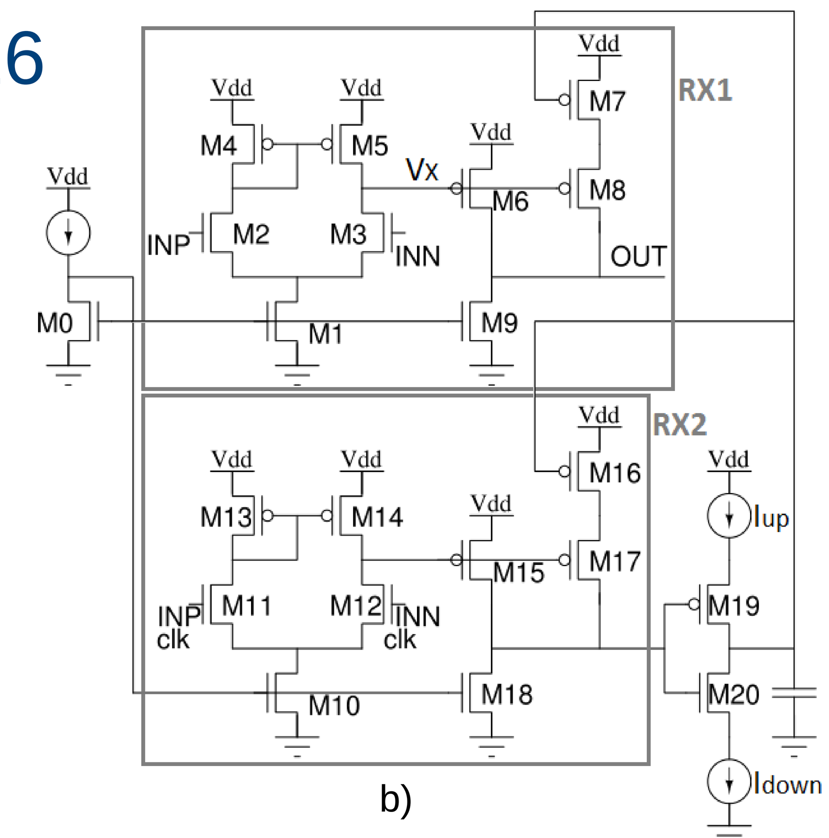
→ duty cycle ≠ 50 %

→ V_{FB} ≠ VDD/2

→ Adjust M7 and M16



a)



b)

Figure 1: LVDS/SLVS receiver with feedback loop: a) Layout b) Schematic

Simulation results

- 2.56 Gbps pseudo random input signal / V_{CM} = 0.8 V
- Small error remains due to CP imbalance

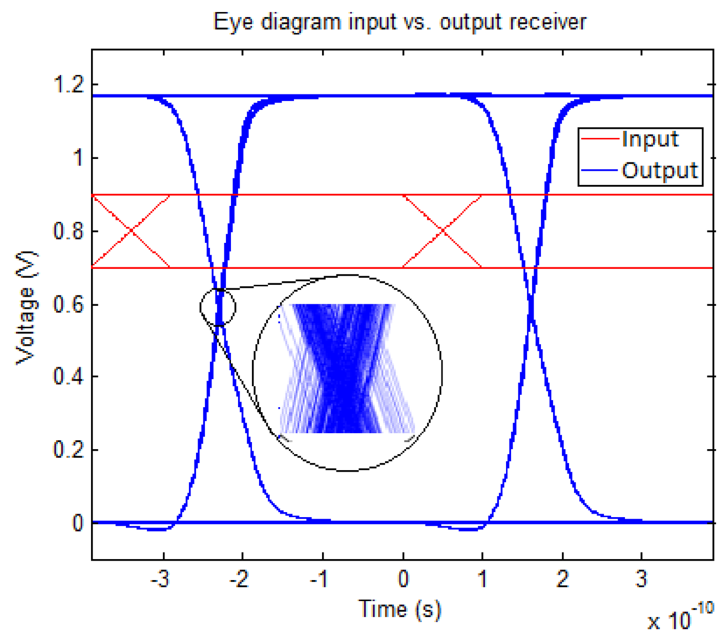


Figure 2: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, $2^7 - 1$ sequence pseudo random bit stream input

Trise / Tfall	100 ps
Crossing voltage	580 mV
Propagation delay	10.3 ns
Propagation delay asymmetry	-1.5 ps
σ_{RMS}	400 fs
Power	500 µW

Table 1: Simulations results LVDS receiver

PVT variations

Process corners	TT	FF	FS	SF	SS
Propagation delay asymmetry [ps]	-1.5	2.2	-5.9	3	-7

→ 10 ps variation

Table 2: Propagation delay asymmetry due to process corners

6.6 ps variation ←

Temperature	-25°C	25°C	85°C	125°C
Propagation delay asymmetry[ps]	-3.6	-1.5	1.5	3

Table 3: Propagation delay asymmetry due to temperature variations

Power supply	1.08 V	1.2 V	1.32 V
Propagation delay asymmetry[ps]	-10.3	-1.5	7.42

→ 17.7 ps variation

Table 4: Propagation delay asymmetry due to power supply variations

Radiation: 500 Mrad models (a)

	With compensation	Without compensation
Propagation delay	17.8 ns	17.9 ns
Propagation delay asymmetry	-1.2 ps	-11.6 ps
Difference vs. normal operation	+ 0.3 ps	+ 13.1 ps

→ 43 times less variation

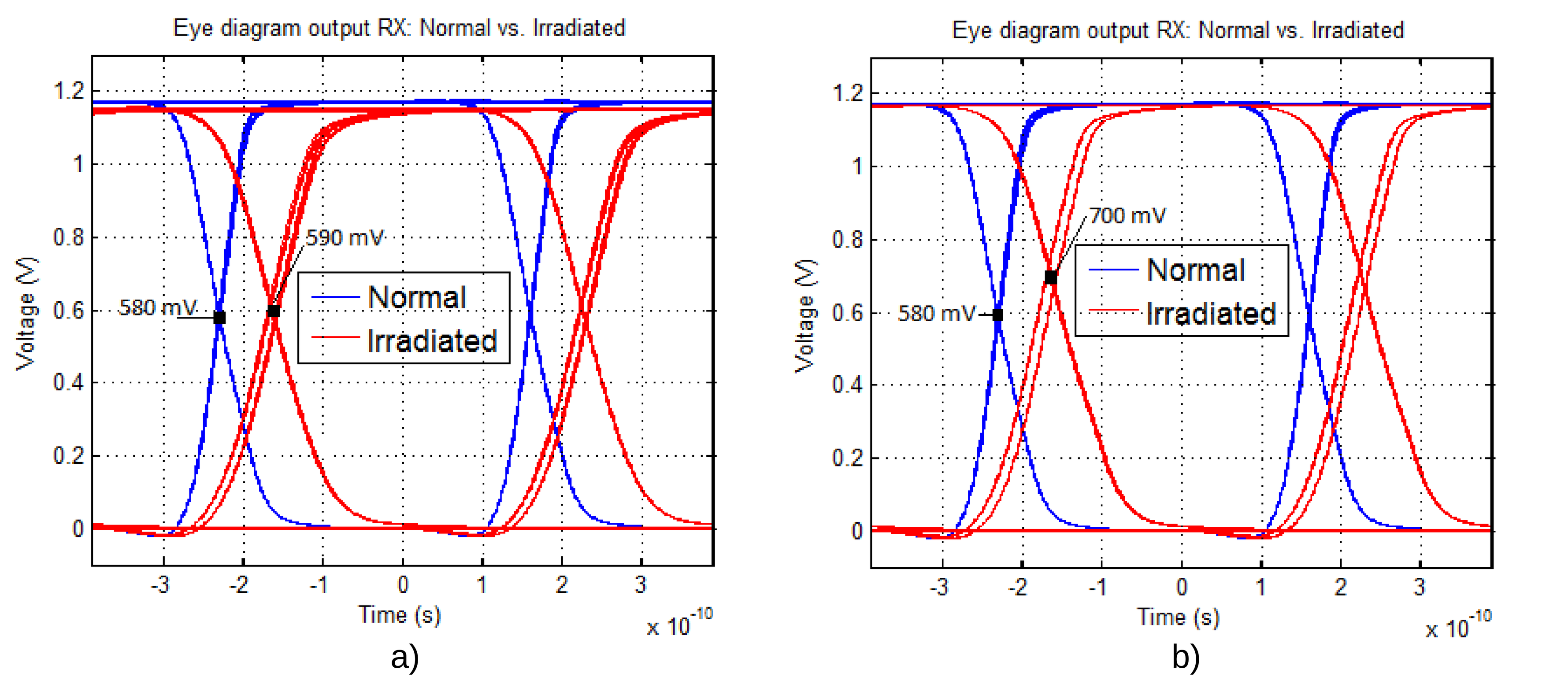


Figure 3: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, $2^7 - 1$ sequence pseudo random bit stream input: a: Normal vs. irradiated output signal with compensation. b: Normal vs. irradiated output signal without

(a) The radiation models have been made available by CPPM (Centre de Physique des Particules de Marseille) through the CERN RD53 collaboration.

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