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Radiation Hardened by Design, Low Jitter, 2.56 Gbps LVDS/SLVS Based Receiver in 65 nm CMOS

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This paper proposes a 2.56 Gbps, radiation hardened by design, LVDS/SLVS like receiver designed in a commercial 65 nm CMOS technology. Simulation results predict 500 µW power consumption and 400 fs RMS output jitter. A replica receiver with a compensation loop is used to measure and compensate variations in the propagation delay of the output edges due to total ionizing dose (TID) radiation effects and/or process-temperature and voltage variations. This loop will ensure an equal propagation delay of the rising and falling output edges, to allow the use in accurate timing circuits.

Summary

Many of today's applications require high precision time-domain signal processing circuits like particle detectors in high energy physics experiments such as the CMS and ATLAS experiments at the Large Hadron Collider (LHC) in CERN or laser-ranging sensors. The key information in these applications is contained in the timing difference between multiple signals or events. This timing information is usually converted to binary data using time to digital converters (TDC). In large and/or complex systems however, the distance between the detector/event generator and the TDC can become rather large, calling for a highly time accurate, long distance, transmission of these signals.

Many applications now use Low Voltage Differential Signaling (LVDS) and Scalable Low Voltage Signaling (SLVS) for data transmission because of its robustness to interferences, low power consumption and high speed. The SLVS standard is comparable to the LVDS standard, with the difference of a 200 mV common mode voltage and 200 mV voltage swing instead of 1.2 V common mode and 400 mV swing. For data transmission applications, the regenerative nature of the receiver allows some tolerance to jitter provided the bit error rate remains low. However, in the envisaged sub-nanosecond timing applications, jitter is the major impairment to the performance of the system. When an LVDS/SLVS receiver is used in the signal path between the event generator circuit and the TDC, any time distortion introduced by the receiver, will cause a time measurement error and consequently will lower the system resolution. An accurate time measurement requires minimal variation in propagation delay for all edges at the output of the LVDS/SLVS receiver.

This paper focuses on the design of a radiation hardened by design LVDS/SLVS receiver which can be used in high resolution time measurement applications. This design uses an NMOS input pair, single ended output op amp structure where the output currents can be tuned in order to achieve an equal propagation delay between the rising and falling edges at the output of the receiver. In radiation environments, the total ionizing dose (TID) will change the gain/propagation delay of the receiver, due to shifts in the threshold voltage and degradation of the charge carrier mobility. This will introduce a propagation delay mismatch between the rising and falling output edges. To compensate this mismatch, a replica receiver is added which is capable of measuring the difference in propagation delay between the two edges. When the propagation delays of the rising and falling edges are equal, an ideal clock at the input of this replica receiver must generate a clock signal at the output with a duty cycle of 50 % and a common mode voltage of VDD/2. Any mismatch in this duty cycle, caused by the TID effects, will be measured by the integrating feedback loop and will be used to adjust the currents through the receiver in order to equalize the propagation delays of the output rising and falling edges.

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