Characterization of radiation effects in 65nm digital circuits with the DRAD digital radiation test chip.

Luis Miguel Jara Casas[1], Davide Ceresa[1], Sandeep Miryala[2], Szymon Kulis[1], Jorgen Christiansen[1], Rui Francisco [1], Dario Gnani[3]

1. CERN – Geneva, SWITZERLAND

2. NIKHEF – Amsterdam, NETHERLANDS

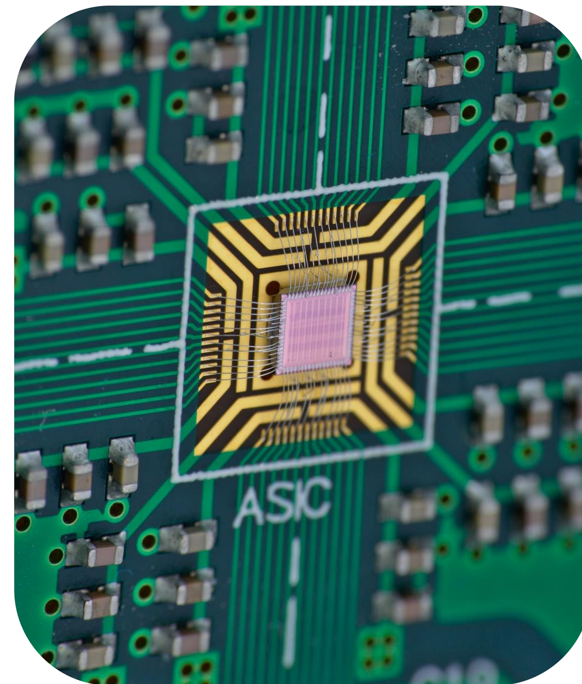
3. BERKELEY LAB – California, EEUU.

Overview

- Studying the impact of high radiation levels on digital electronics in 65nm CMOS technology is vital for key sub-detectors of the ATLAS and CMS upgrades. A **Digital RADiation (DRAD)** test chip has been specifically designed to study the **impact of Total Ionizing Dose (TID)** (< 1 GRad) and Single Event Upset (SEU) on digital logic gates in a **65nm CMOS technology**.
- Nine different standard cell libraries are studied in this chip, differing in the transistor dimensions, V_t flavour and layout of the device.
- Each library has eighteen test structures specifically designed to **characterize delay degradation** and power consumption of the standard cells. For SEU study, a dedicated test structure based on a shift register is designed for each library.

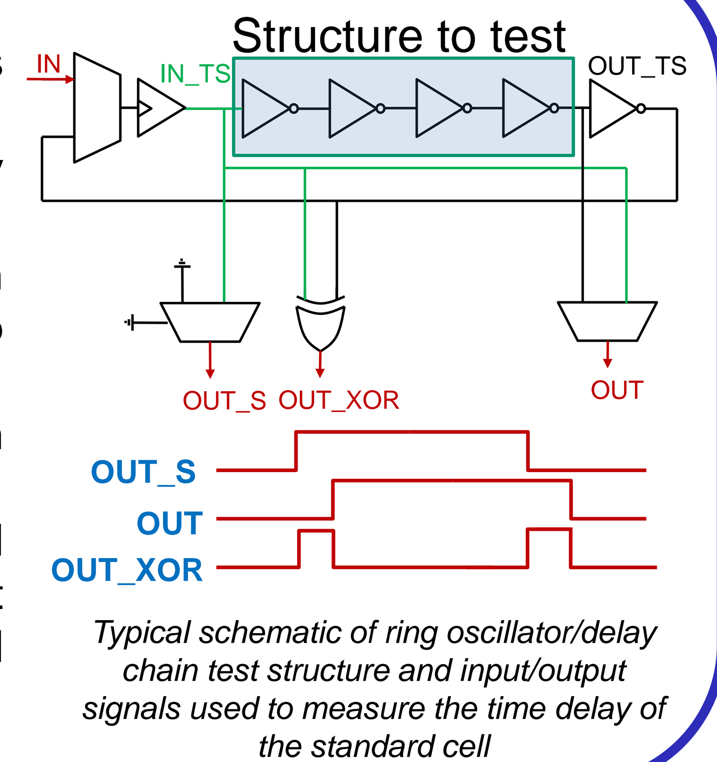
Description of DRAD chip

- **9 digital libraries** are included, with different properties:
  - Number of tracks: 7, 9, 12 and 18 tracks (identified as **7T**, **9T**, **12T** and **18T**)
  - V_t flavours: normal (**NVT**), low (**LVT**) and high (**HVT**) V_t (threshold voltage).
  - Device dimensions, increasing transistor length (**12T_NVT_2L** has transistors of 130nm instead of 60nm, 2x longer respect 12T_NVT) and width (internal transistors of sequential cells of **9T_NVT_2W** have a width of 300nm instead of 150nm, 2x wider than 9T_NVT).
  - 18 track library is made with **enclosed layout**.
- Each library is composed of ten combinational cells and two sequential cells.



DRAD chip. 2x2 mm² mini@sic.

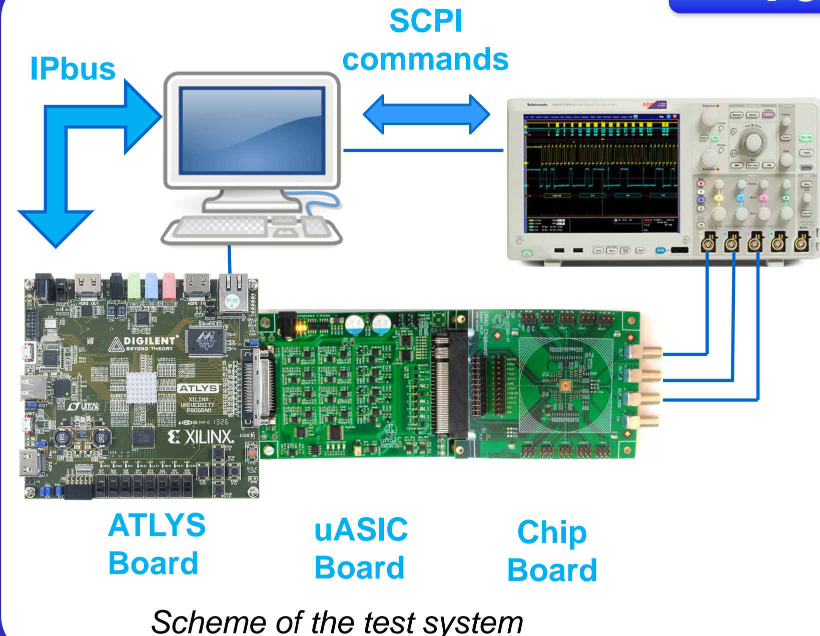
- Delay degradation for various gates (NAND, NOR, XOR, buffers and inverters, flip-flop and latch) is measured using delay chain and ring oscillator test structures.
- Dedicated test structures have been designed for the measurement of setup and hold time.
- A long shift register is implemented in each library for Single Event Upset (SEU) study.
- Specific high speed structures (VCO and counters) are included only for the fastest library (18T_LVT) for future high speed optical link chips.



Typical schematic of ring oscillator/delay chain test structure and input/output signals used to measure the time delay of the standard cell

Test system and X-RAY facility

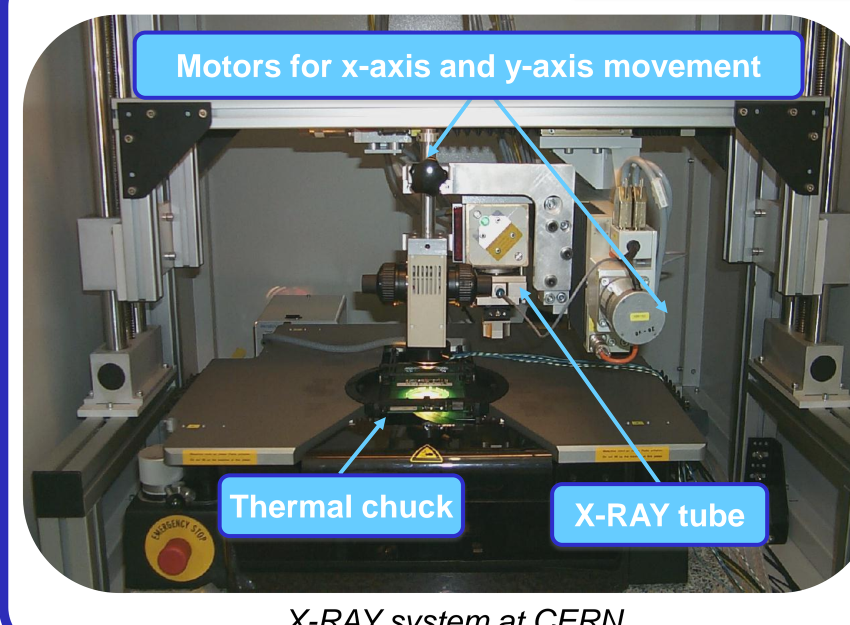
Test system



Scheme of the test system

- A test system has been developed based on an Atlys evaluation board, an interface board (uASIC board) in charge of powering the chip, power monitoring and the conversion between signaling standards, and a small carrier board with a wire bonded DRAD chip.
- Delay characterization is performed with an external high speed sampling oscilloscope.
- IPbus protocol is used for computer-FPGA communication .
- Communication with oscilloscope is done via SCPI.

X-RAY facility



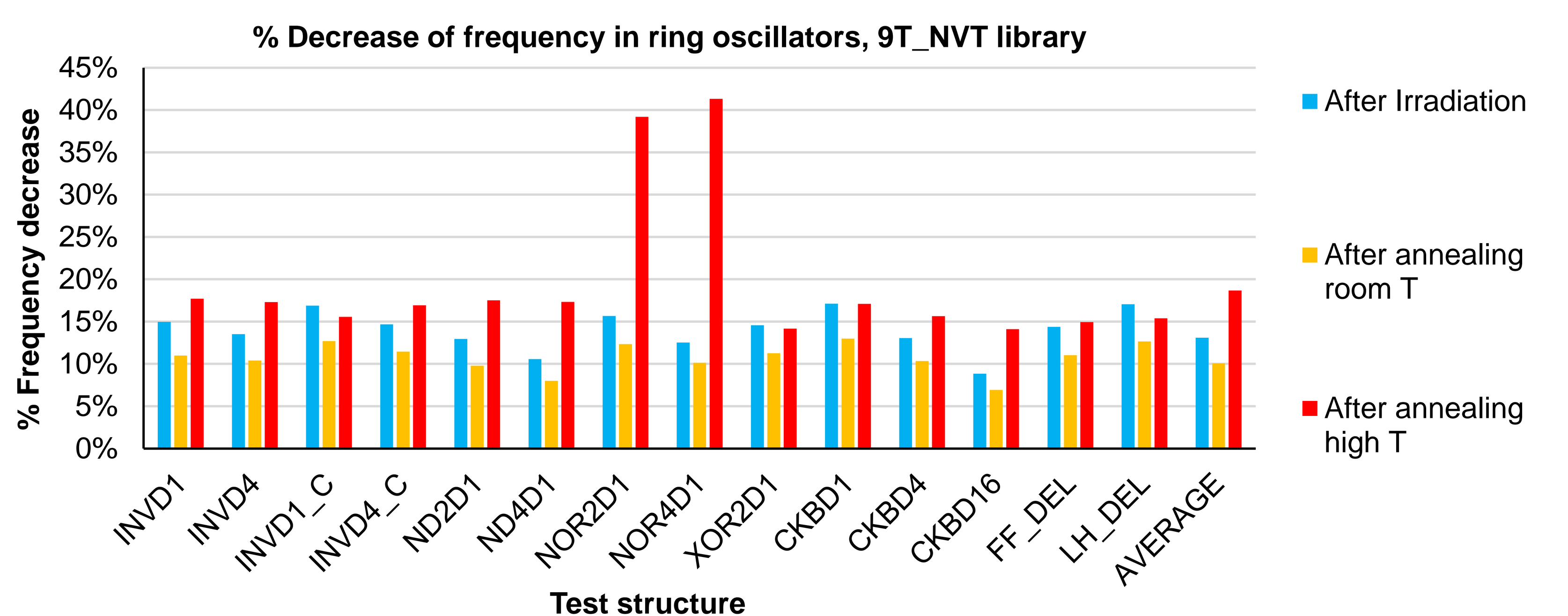
X-RAY system at CERN

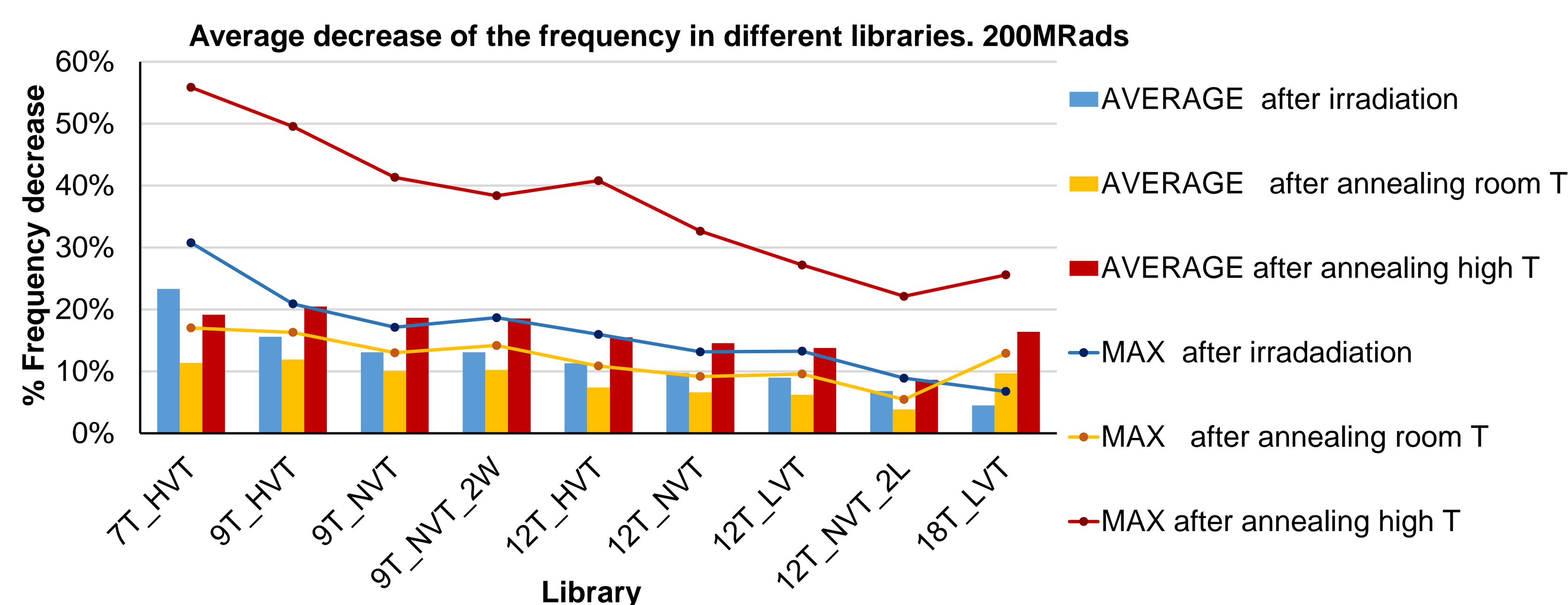
- Total ionization dose radiation tests have been done in the X-RAY facility at CERN. Tests were done at **high dose rate** (9 MRads/h).
- Test structures are dynamically changing during irradiation in order to keep each gate in a different state half of the time.

Results

200MRads, room temperature

- First results of the testing for a total ionizing dose of **200 MRads** at **room temperature** are shown.
- After irradiation, the chip was **annealed** at **room temperature** during **one week** followed by **high temperature (100°C)** annealing.



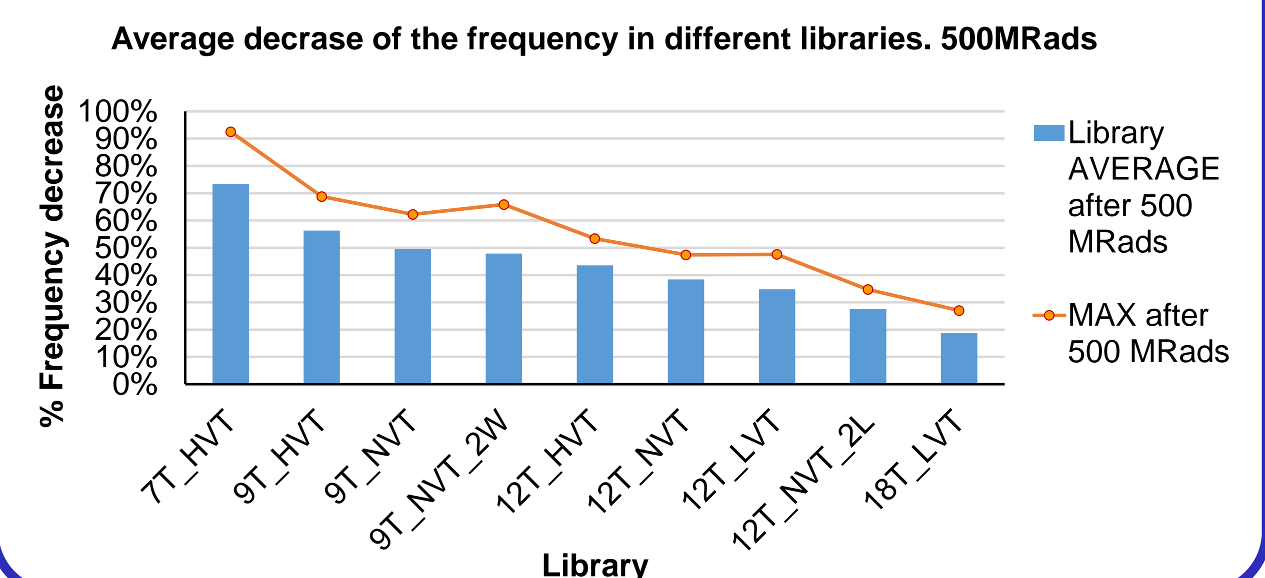


- *All gates present a small improvement after room temperature annealing and a worsening after high temperature annealing .*
- *NOR gates have the highest degradation due to the fact that the PMOS transistors present worse behavior after irradiation than NMOS transistors.*
- *The behavior relationship between different libraries is as expected: libraries with smaller size present bigger degradation and, between libraries with the same size, those with higher V_t behave worse than libraries with lower V_t.*
- *12T_NVT_2L is intrinsically slower than 12T_NVT.*

- After annealing at room temperature most of the libraries behave better, but after **high temperature annealing** the **delay** of the gates **increases significantly**.

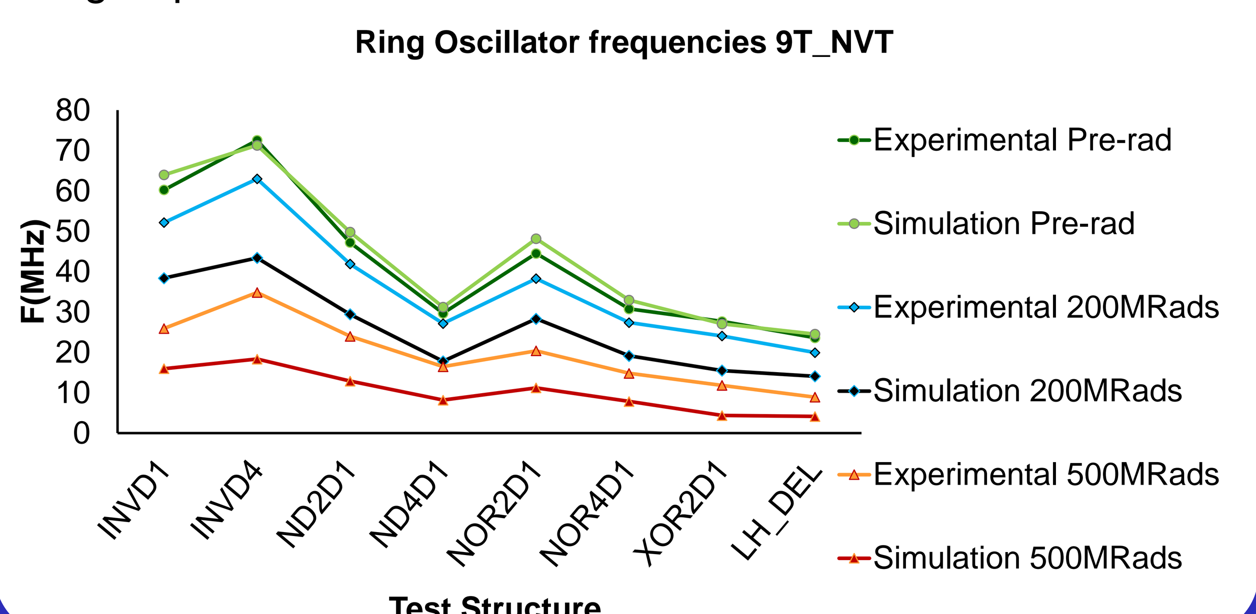
500MRads, room temperature

- A second irradiation campaign was done reaching **500 MRads** at **room temperature**, results after irradiation are shown (results after annealing not yet available):



Comparison with simulations

- **Simulations** were done using **200 MRads and 500 MRads transistor models** from the radiation working group of the RD53 collaboration.



Summary

- A digital radiation chip (DRAD) has been designed and tested in order to characterize the delay degradation of standard cells in a 65nm technology, using several libraries with different properties.
- Some of the results obtained and comparisons with simulations are shown.

Future work

- New irradiation campaigns varying the temperature and total ionizing dose are ongoing and will be done in the next months, as well as SEU testing.

Contact person: LUIS MIGUEL JARA, luis.miguel.jara.casas@cern.ch