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Characterization of Radiation Effects in 65nm Digital Circuits with the DRAD Digital Radiation Test Chip

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A Digital RADiation (DRAD) test chip has been specifically designed to study the impact of Total Ionizing Dose (TID) (< 1GRad) and Single Event Upset (SEU) on digital logic gates in a 65nm CMOS technology. Nine different versions of standard cell libraries are explored in this chip, basically differing in the device dimensions, Vt flavor and layout of the device.
Each library has eighteen test structures specifically designed to characterize delay degradation and power consumption of the standard cells. For SEU study, a dedicated structure based on a shift register is designed for each library.
First irradiation results will be presented.

Summary

Radiation effects concerning on-detector electronic systems are one of the main challenges for the ASIC design engineers. The unprecedented radiation environment considering HL-LHC detector upgrades requires significant investigation of very high total ionization dose effects not only on the single MOS device alone but also on the digital logic gates.
Studying the impact of high radiation levels on digital electronics in 65nm CMOS technology is vital for key sub-detectors of the ATLAS and CMS upgrades. ATLAS and CMS pixel detector chips (RD53 collaboration) require radiation tolerance of up to 1Grad for a 10 years lifetime for the inner layers of the vertex detectors. Outer tracker detectors require radiation tolerance of the order of 100Mrad (e.g. the MPA chip for the CMS tracker upgrade) and high speed optical link chips for LPGBT, require very high circuit speeds after radiation damage.
The aim of the DRAD chip is to measure the delay degradation under different TID on different customized libraries composed of ten combinational and two sequential cells each. These libraries differ in minimum device dimensions (both L and W), type of transistors (Normal Vt, Low Vt and high Vt) and layout of the device (normal and enclosed).
The delay degradation is measured using test structures (delay chains and ring oscillators) with different gates (NAND, NOR, XOR, buffers and inverters, flip-flop and latch) for each of the standard cell library. To deal with sequential elements, specific structures have been designed to the measurement of setup and hold time. In addition a 24 bit synchronous counter is included for the study of radiation effects in a typical digital composite circuit. To study the effect of SEU, a large shift register is implemented in each library. High speed structures (VCO and counters) are included only for the fastest library which has enclosed layout and low Vt transistors for future high speed optical link chips. The test structures have been optimized and verified using 200 and 500MRad transistor models from the radiation working group of RD53 collaboration.
A small and portable test system has been developed for the DRAD chip to enable radiation tests to be performed in X-ray facilities, and it can be adapted for other radiation test facilities (Cobalt, Ion beam, Proton beam). The test system is based on a Spartan 6 FPGA evaluation board, an interface board in charge of powering the chip, power monitoring and the conversion between signaling standards, and a small carrier board with a wire bonded DRAD chip. Delay characterization can be performed with a TDC function integrated in the FPGA and/or with the help of an external high speed sampling oscilloscope.

The DRAD chip, a 2x2 mm mini@sic, was submitted on March 23 2016 and is expected to be available by the end of May. The test system is in the process of final stage of implementation. The X-ray radiation tests will be carried out this summer, and the measurement results will be presented at the TWEPP workshop.

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