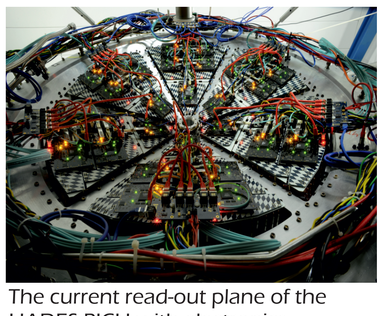
Electronics for the RICH detectors of the HADES and CBM experiments

Jan Michel[1], Mike Faul[2], Jürgen Friese[3], Karl-Heinz Kampert[4], Vivek Patel[4]
Christian Pauly[4], Dennis Pfeifer[4], Peter Skott[2], Michael Traxler[2], Cahit Ugur[2]
[1] Goethe Universität Frankfurt, [2] GSI Darmstadt, [3] TU München, [4] Bergische Universität Wuppertal

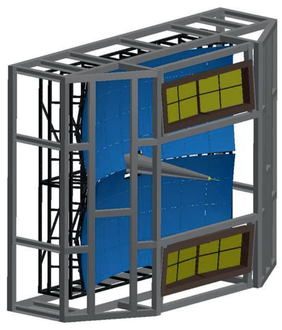
The RICH detectors

HADES RICH
- operational since 2000 @ GSI
- 1.2 m² detector surface
- 28,000 channels
- CsI cathode to be replaced by PMT

CBM RICH
- to be finished in 2020 @ FAIR
- 2.8 m² detector surface
- 60,000 channels
- 10 MHz collision rate
- up to 200 GBit/s



The current read-out plane of the HADES RICH with electronics



CAD model of the CBM RICH height 5 meter

Collaboration

Common Challenges
densly packed channels, 3 px/cm²
small single-photon signals
timing precision ~ 100 ps

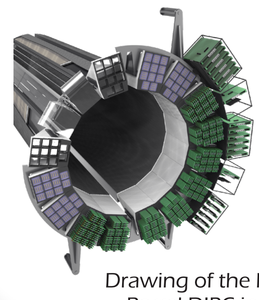
Savings in Collaboration
PMTs will be used in both detectors
Major parts of electronics identical

Design Policy

all electronics fit to back of PMTs
small modules for flexibility
use dedicated, discrete amplifiers
in-FPGA time measurement
low power to ease cooling
modular design to separate functions
use space efficiently
as few cables as possible

Panda DIRC

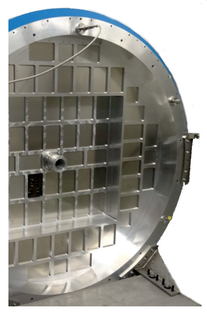
Same scheme is planned for the Panda Barrel DIRC
- MCP-PMT (better timing, magnetic fields, 2x smaller signal)
- 11,000 channels
- similar rates to CBM

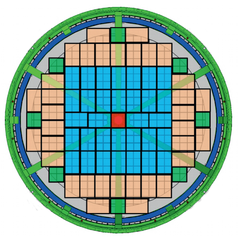


Drawing of the PANDA Barrel DIRC including electronics

This project makes use of the developments made within the TRB collaboration during the past years contributed by people from various institutes and experimental groups

Assembly



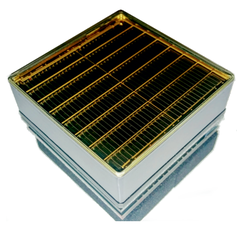


The new HADES RICH backplane fitted with 74 read-out modules

Components
- MAPMT carrier backplane
- Analog & TDC front-end card
- Data concentrator for DAQ connection
- Power supply card
- Connectivity: power, optical, HV
  - Optional: clock, trigger

Rate Capabilities
- Electronics > 5 MHz/channel
- Data links > 20 MHz/module
  - optional trigger windows
- CBM: up to 200 kHz/channel or 60 MHz/module
  - Needs data concentrator upgrade

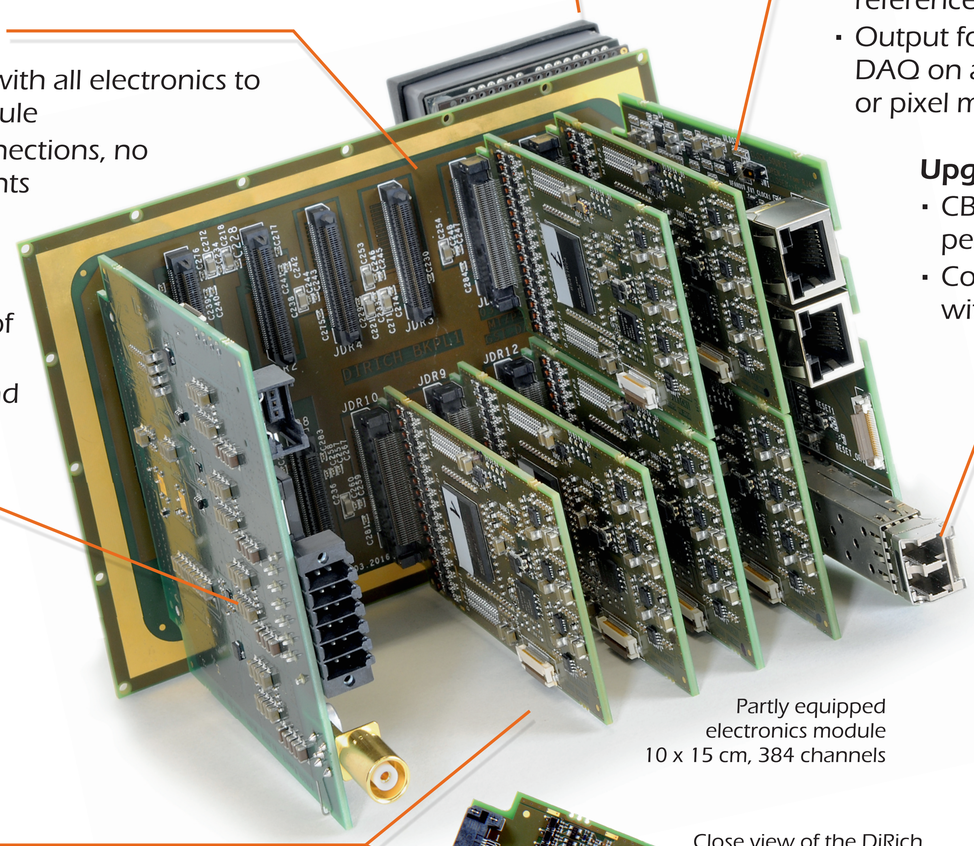
Photo Multiplier



- Multi-Anode PMTs
- Hamamatsu H12700
- 64 Pixel, 6 x 6 mm² each
- sensitivity 200 - 600 nm
- single photon efficiency >30%
- timing 300 ps (TTS)

Backplane

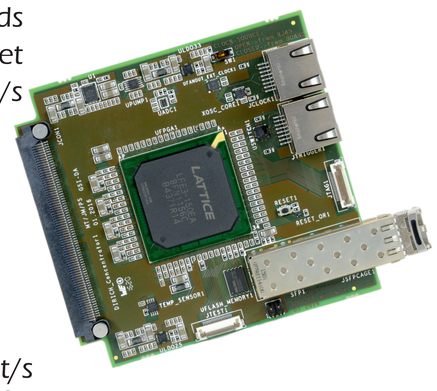
Combines 6 PMT with all electronics to one read-out module
- all electrical connections, no active components
- light & gas-tight shield
- complex design due to number of connections
- mix of analog and digital signals



Partly equipped electronics module
10 x 15 cm, 384 channels

Data Concentrator

- Lattice ECP3-150 FPGA
- Bi-directional links to all 12 front-ends
- Event data is merged into one packet
- Optical link to central DAQ 2.4 GBit/s
- Inputs for external clock and reference time
- Output for trigger signal to run DAQ on any coincidence or pixel multiplicity



Upgrade Options
- CBM data rates exceed 5 GBit/s per module in central parts of the detector
- Concentrator replaced independently with new module with 1/2 4.8 GBit/s links

Power Board
- DC/DC converters to produce all required voltages
- Option: direct supply without converters for noise reduction (to be quantified)
- Voltage and current monitoring

- Power dissipation: about 25 W per module
- Total power consumption: about 2 kW (HADES)

Data Transport

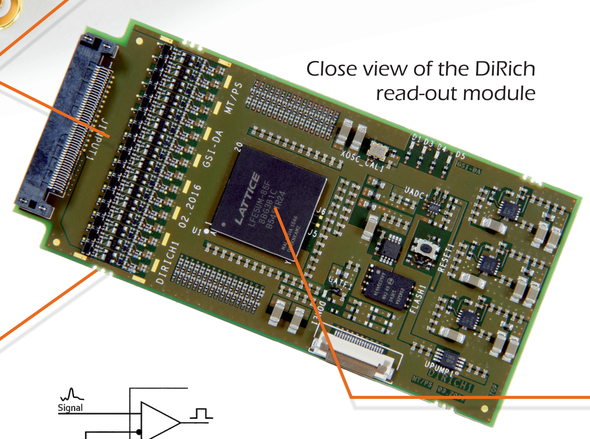
All communication is transported over TrbNet, the HADES DAQ network protocol
- Trigger / Synchronization
- Event data
- Slow Control
- 2 GBit/s LVDS (backplane) or optical fiber

Further data aggregation in hubs based on TRB3 boards

Forwarded to server farm via GbE

Front-end Board
- Each PMT is read out by two front-end cards
- 32 analog channels
- Local linear voltage regulators
  - ultra-low drop (< 40 mV)
- 47 x 100 mm

FPGA (Lattice ECP5-85)
- Thresholds
  - internal Delta-Sigma-DAC + Filter
- Discrimination
  - comparator in LVDS receivers
- Time Measurement
- DAQ logic - Read-out, Triggering



Close view of the DiRich read-out module

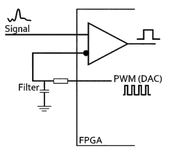
Read-out Modes

HADES	CBM
triggered DAQ	free running DAQ
merging of data based on event numbers	merging of data based on time slices
centrally controlled read out	free-streaming
	synchronuous clocking

Systems based on same low-level network with Identical features for slow-control, monitoring ...

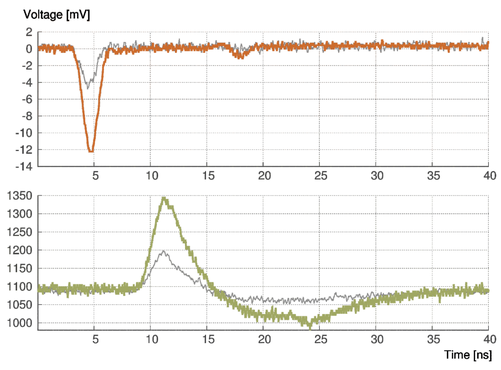
Analog Stage

low power shaping amplifier
discrete off-the-shelf components

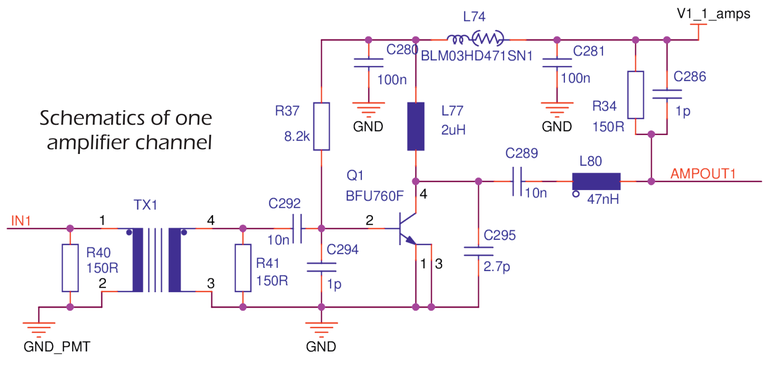


FPGA-based discriminator

- small footprint: 12 x 2.7 mm²
- mostly 0201 (0603 metric) components
- 12 mW @ 1.1 V
- Amplification ~ 20 - 30 depending on amplitude
- Channels galvanically isolated
- threshold ~ 1 mV of input

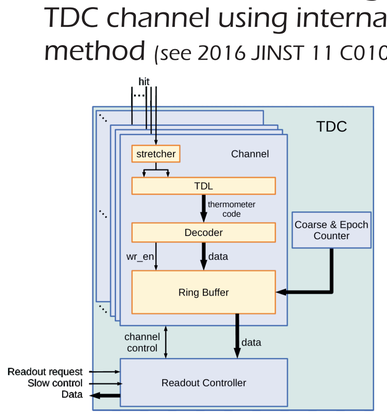


Example signals. Top: Input, Bottom: Output
Shown are two typical PMT signals with 12 mV and 4 mV amplitude

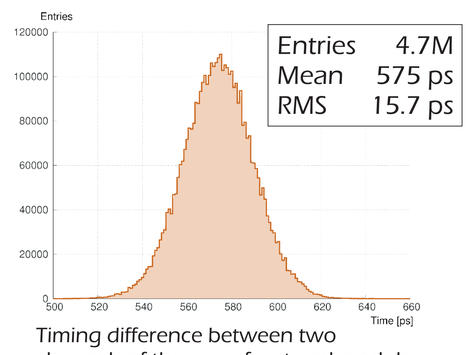


Schematics of one amplifier channel

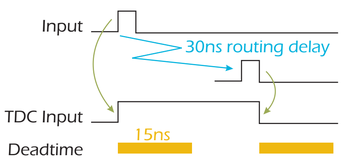
Time Measurement
- Timing precision ~ 20 ps
  - PMT timing ~ 300 ps
  - high precision needed for ToT (amplitude, e.g. double hits)
- Measurement of both edges in same TDC channel using internal stretcher method (see 2016 JINST 11 C01046)



Architecture of the in-FPGA TDC



Timing difference between two channels of the same front-end module



The falling edge of the input can not be detected due to the intrinsic dead-time of the TDC. Instead, routing is used to delay the falling edge until the TDC is ready again.

Photography: G. Otto (GSI)
Contact: michel@physik.uni-frankfurt.de
TRB collaboration: http://trb.gsi.de

This work is supported by GSI and BMBF grant 05P15PXFCA