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Electronics for the RICH Detectors of the HADES and CBM Experiments

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The RICH detectors of the existing HADES spectrometer and the CBM experiment (to be built at FAIR) will use 64 channel Multi-Anode PMTs.
We designed a complete set of digitizing electronics, consisting of analog and digital frontend modules, power supply and data concentrator cards plugged into a backplane carrying 3x2 MAPMTs on the front side, and all readout modules on the backside.
These contain all necessary supply electronics, preamplifiers and FPGA-based TDC as well as the digital data and trigger handling logic and an optical transceiver. We are going to present the electronics along with performance test results.

Summary

The heavy ion spectrometers (HADES and CBM) at the GSI Helmholtz Center for Heavy Ion Research (Darmstadt, Germany) and the FAIR accelerator contain a RICH
detector for particle identification. The existing RICH at the HADES experiment is in operation since the year 2000 and is currently being
upgraded with a new MAPMT readout plane consisting of 428 64-channel PMTs (Hamatsu H12700). Here we designed a set of read-out
electronics which are to be used in the CBM experiment as well,
and which is also planned to be used by the Barrel DIRC detector
of PANDA with an adaption to the backplane design.

The major components of the read-out solution are the backplane, front-end modules
a data combiner and power supply. Each building block consists of 6 PMTs and all
required electronics constrained to a volume of 10 cm times 15 cm times 15 cm. The backplane is used
as a mounting and interconnect structure for all modules as well as to separate the radiator gas volume from the
ambient atmosphere. Front-end modules contain a discrete, low-power amplification
stage (< 10 mW per channel) as well as FPGA-based 32 channel TDC (utilizing a Lattice ECP5 FPGA with 85k LUTs).
These provide a leading
and trailing edge time measurement precision with an RMS well below 100 ps with on-chip calibration, while the single edge time precision including external calibration is about 10 ps RMS.
Data from all 6 PMTs (384 channels) is then transported from the front-end modules
via the backplane to a data concentrator card based on a Lattice ECP3 FPGA. From here
a 2 GBit/s optical link (common to all subsystems in the HADES detector) receives trigger
information and sends all event data to a server farm.

On all inter-FPGA links the
TrbNet protocol used throughout the HADES detector is used to ensure proper trigger and busy
handling, data transport as well as extensive slow control capabilities. Last part of the electronics
is the power supply module that allows to power each submodule with all voltages needed.
The total power of the assembly is about 20 Watt (6 PMT / 384 channels).
The modular electronics allow for a simple adaption of the read-out modules to

the high data rates expected for the CBM experiment. In the region of highest occupancy, the data concentrator cards will be replaced with a more capable FPGA and use one or two 4.8 GBit/s optical links. The total data rate of the system will sum up to about 200 GBit/s at an envisioned collision rate of 10 MHz Au+Au.

We are going to present the concept of our very compact electronics setup along with test results regarding precision and noise figures.
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