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The Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS Muon Upgrade

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The ART Data Driver Card (ADDC) will be used in the ATLAS New Small Wheel (NSW) upgrade to process and transmit the Address in Real Time (ART) signals, which indicates the address of the first above-threshold event. A custom ASIC (ART ASIC) will receive the ART signals and do the hit-selection processing.
To evaluate the performance of the ADDC before the ART ASIC is fabricated, an FPGA based prototype is built. A Xilinx Artix-7 FPGA is used to emulate the ART ASIC. The bench test results of this prototype including performance and latency measurements will be described.

Summary

The ART Data Driver Card (ADDC) is designed for the Micromegas detector in the ATLAS New Small Wheel (NSW) to transmit the trigger data from the front end ASICs to the trigger processor in the USA15. For the Micromegas detector, the trigger primitive is the Address in Real Time (ART). The ART is generated by each of the 64-channel front end ASIC (the VMM) at every bunch crossing and it is the 6-bit address of the strip with the earliest hit above a given threshold. The ADDC receives the ART signals from the front-end board, does a priority-based hit selection, and then sends the selected data to the back end trigger processor. The hit selection will be processed by a custom ASIC, the ART ASIC. Finally the GBTx ASIC and VTTx transmitter module collect data from up to 32 front end ASICs and transmit them to the trigger processors through an optical fiber link. To take advantage of the dual optical transmitter links on one VTTx module, the ADDC board is designed to handle 64 front end ASICs with 2 GBTx chips. Another ASIC of the GBT chipset, the GBT-SCA, will be used on the ADDC for configuration and control of the ART ASIC and the second GBTx.
Since the ART ASIC is not yet available, to evaluate the performance of the ADDC, an FPGA-based prototype has been built at a smaller scale. This prototype includes most of the major functional components of the final ADDC while a Xilinx Artix-7 FPGA is used to emulate the ART ASIC. This prototype has half density of the final version ADDC, with one FPGA and one GBTx chip on board, and it can handle 32 channels of ART data. Although the ART ASIC itself is not available, the design group has provided the HDL code of the ASIC in advance so we could port it in the FPGA and implement the hit-selection algorithm. Compared to the VTTx module for the final ADDC, this prototype uses the VTRx module, which has 1 transmitter for the uplink data transmission and 1 receiver for the down link configuration.
Several tests have been carried out to verify the functionality and stability. The FPGA evaluation board KC705 is used to communicate with the prototype. An ART pattern generator (APG) that can emulate the ART data output of 32 VMM front-end ASICs simultaneously has been developed by the Harvard group. In the integration test, Micromegas hits from an ATLAS New Small Wheel simulation are fed into the APG, the FPGA based ADDC prototype receives and processes the 32-channel ART data, and the results are sent to the MM trigger processor prototype. The evaluation test results of the integration readout chain, including reliability studies, latency and overall performance will be reported.

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