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A PCI DAQ Board Prototype after the ATLAS Pixel Detector IBL-Layer 1 and 2 ROD Cards

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The ATLAS Pixel detector has inserted an additional inner layer called Insertable B-Layer (IBL) that is read out via two boards: the Readout-Driver card (ROD) and the Back-of-Crate card (BOC). In this presentation we summarize first the experience of building and commissioning the boards to read out the ATLAS Pixel detector, with particular emphasis to the ROD card.
In addition, here it is presented the design and the preliminary tests of a prototype card, backward compatible with ATLAS Pixel Detector, which also features PCI express and GBT and other I/O interfaces.

Summary

This paper summarizes first the experience of designing, building, testing and commissioning the boards to read out the ATLAS Pixel detector, with particular emphasis to the ROD card.
The current ATLS Pixel Detector is composed in particular of four layers: IBL, B-Layer, Layer 1 and Layer 2. Except the B-Layer, the others have been equipped with a new generation of VME readout cards to improve the readout speed and to interface with the new IBL detector.
However, for the upgrade of the LHC experiments, the pixel detectors will need electronics with additional features to interface with newer readout systems. The prototypes are intended to extend the capabilities of the current ATLAS Pixel Detector readout system and this is why we planned to design a new readout board backward compatible to the pixel detectors, compatible to the current readout firmware, plus extendable to future features such as being interfaceable with PCI express and GigaBit Transceiver (GBT) ports. In this way the board can connect to optical fibers like those implemented in the LHC experiments to read out front-end silicon detectors and, at the same time, is able to interface with commercial GPU boards, which use PCI ports at very high speed. The new design features modern FPGA generations (Kintex and Virtex-7) to maximize the potential of the internal soft-core blocks, like transceivers and parallel-to-serial converters. Also, a commercial processor (ARM family) will be used to run all the embedded software currently implemented into the IBL ROD firmware.

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