The Versatile Link Demo Board (VLDB)

R. Martín Lesma, J. Barbosa, S. Baron, C. Caplan, P. Leitao, C. Pecoraro, D. Porret, K. Wyllie

EP-ESE-BE Section, CERN, 1211 Geneva, Switzerland

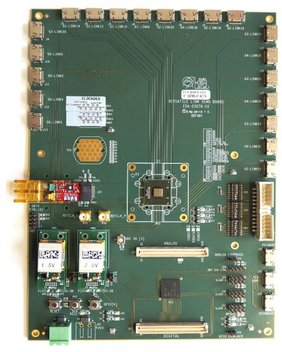
Abstract

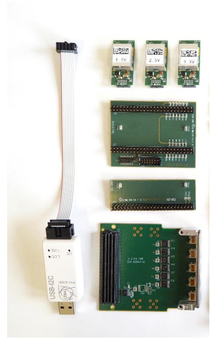
The Versatile Link Demonstrator Board (VLDB) is the evaluation kit for the Radiation Hard Optical Link ecosystem, which provides a 4.8 Gbps data transfer link for communication between front-end (FE) and back-end (BE) of the experiments. It gathers the Versatile Link main radiation hard custom ASICs: GBTx, GBT-SCA and VTRx/VTTx plus the FeastMP, a radiation hard in-house designed DCDC. This board is the first design allowing system-level tests of the Link with a complete interconnection of the constitutive components, allowing DAQ, control and monitoring of FE devices with the GBTx – SCA pair.

The VLDB and its Components

The VLDB is a demo board which includes only radiation hard qualified components. These components are:

- GBTx: Gigabit Transceiver ASIC dedicated to serialization, deserialization, FEC and data and clock recovery.
- GBT-SCA: ASIC dedicated to slow control and status monitoring of the front-end modules (FE). It can handle up to 16 I^2C, 8 SPI and 1 JTAG slaves, plus 32 GPIO lines, 31 ADC analog inputs and 4 DAC channels.
- VTRx/VTTx: optical transceiver/dual transmitter. The VLDB can also work with a commercial SFP+.
- FEAST MP: DCDC converters supplying 1.5V and 2.5V/3.3V to both on-board components and VTRx/SFP+.

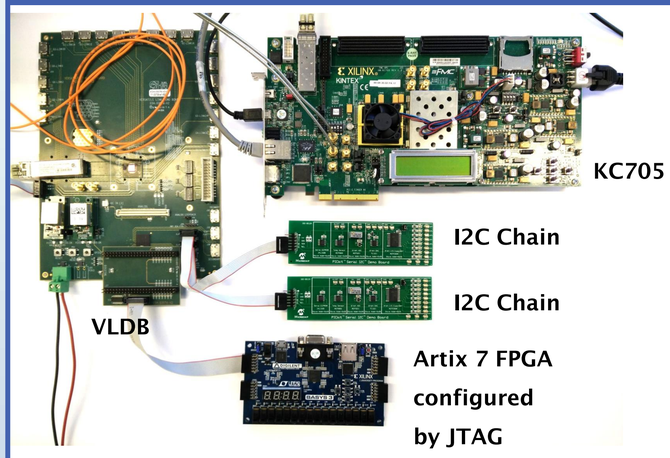




The VLDB can be used to :

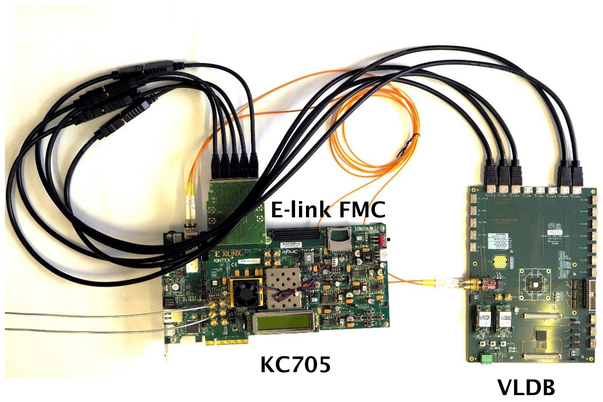
- Gain expertise on the complex set of configurations provided both by the GBTx and by the SCA.
- Characterize the radiation hard optical ecosystem, in particular focusing on the recovered clock delivered to the FE.
- Test firmware and software implementations of back-end.
- Test the communication with up to 20 front-end modules via e-link/HDMI ports.
- SEU and total dose radiation tests.
- Be a reference board for the design of experiments front-end boards.

Testing the GBT and its Ecosystem

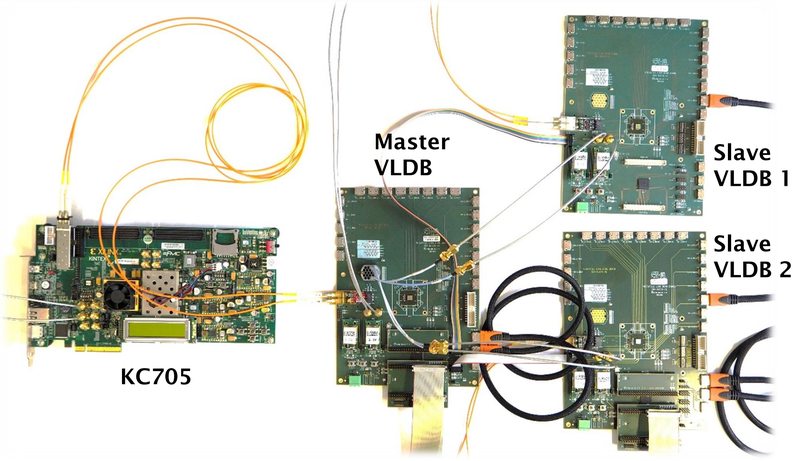


The picture above shows an example of SCA test setup* which depicts two I^2C demo boards and one FPGA used as slaves from the SCA. In this setup the KC705 sends data through the EC field of the GBT serial frame. The Artix 7 FPGA can be configured through the JTAG link controlled by the SCA.

* The connections in this picture are voluntarily simplified.



This picture shows a setup which consists of a VLDB, a KC705 board (acting as back-end board), an optical link and a 5 e-link connection through HDMI cables and an e-link FMC. In this way data can be serialized by the GBT-FPGA in the Kintex 7, transmitted over the optical link, recovered by the GBTx, distributed on the e-links and checked back in the FPGA.



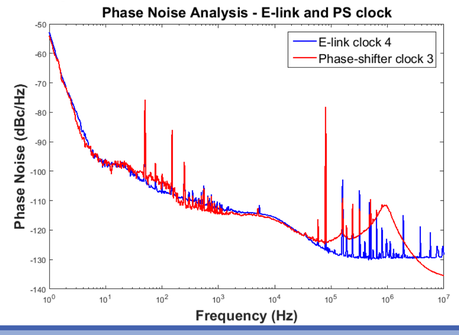
The picture below depicts another example of SCA test setup. It shows a VLDB (centre) acting as a master and the two other (right) as slaves. The master VLDB gets configured from the optical link, while the other two get their configuration from the I^2C links coming from the master SCA. The slaves also get the reference clock from the GBTx of the master VLDB. The full setup is controlled by the KC705 on the left, and several slave devices -not shown here- can be controlled from the SCAs on the slave VLDBs.

Jitter & Phase Studies

In the VLDB the clock is recovered from the versatile link, and can then be provided to other boards or setups. There are two ways to deliver the clock

- Via the 8 phase-shifter clock outputs (Desclk) on the Bull's eye connector.
- Via the 20 e-link clock pairs (available on HDMI ports).

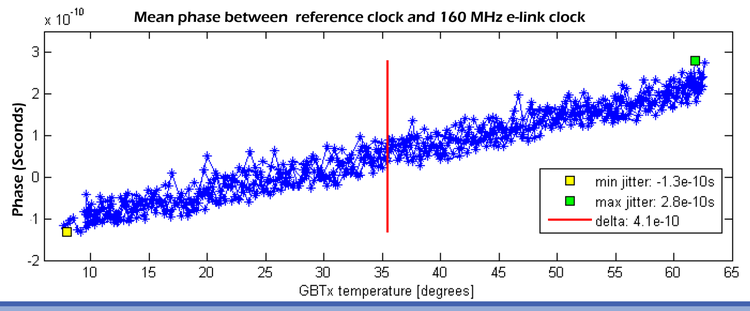
The random jitter of the Desclk outputs is slightly higher (around 15 ps rms in the best case) due to the impact of the phase-shifter chain. E-link clock random jitter is typically of the order of 10 to 12 ps rms. See below the phase noise plot of one e-link and one phase-shifter clock outputs.



A temperature test has been conducted on the recovered clock from the VLDB, measuring the jitter variation with the temperature. The setup uses a climate chamber to change the ambient temperature in which the GBTx is placed and reset every 30 seconds.

The phase of different recovered clocks (phase-shifted clocks, e-link clocks and internal clocks) has been tracked with respect of the clean reference clock provided by a CG635 generator and feeding the GBT-FPGA transceiver.

The results show a phase linearly drifting by typically a few hundreds of picoseconds for temperatures going from 5 to 65 degrees. No phase jump has been detected over tens of thousands of reset cycles. As an example, the phase variation at 160 MHz is showed in the figure below .

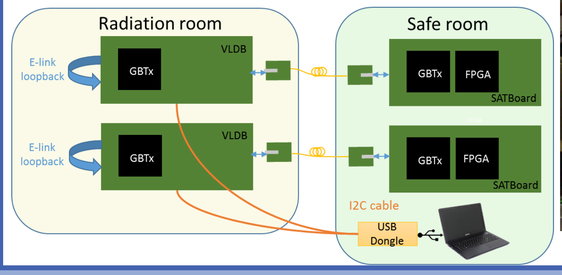


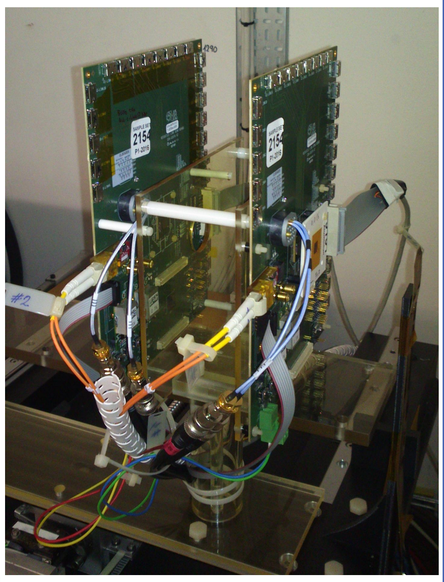
Radiation Tests

A total dose radiation test was done in the IRRAD1 installations at CERN. The aim of this test was to evaluate the Total Ionizing Dose (TID) that the full system could sustain.

Two VLDBs were set in the centre of the beam trajectory, receiving directly the impact from protons from the PS accelerator. The registers in the GBTx were read continuously to check the corrections made internally.

The setup withstood up to 400 MRad in working conditions, although the link unlocked in every proton spill, due to the very high energy of each spill (approximately 2.5 KRad per spill).



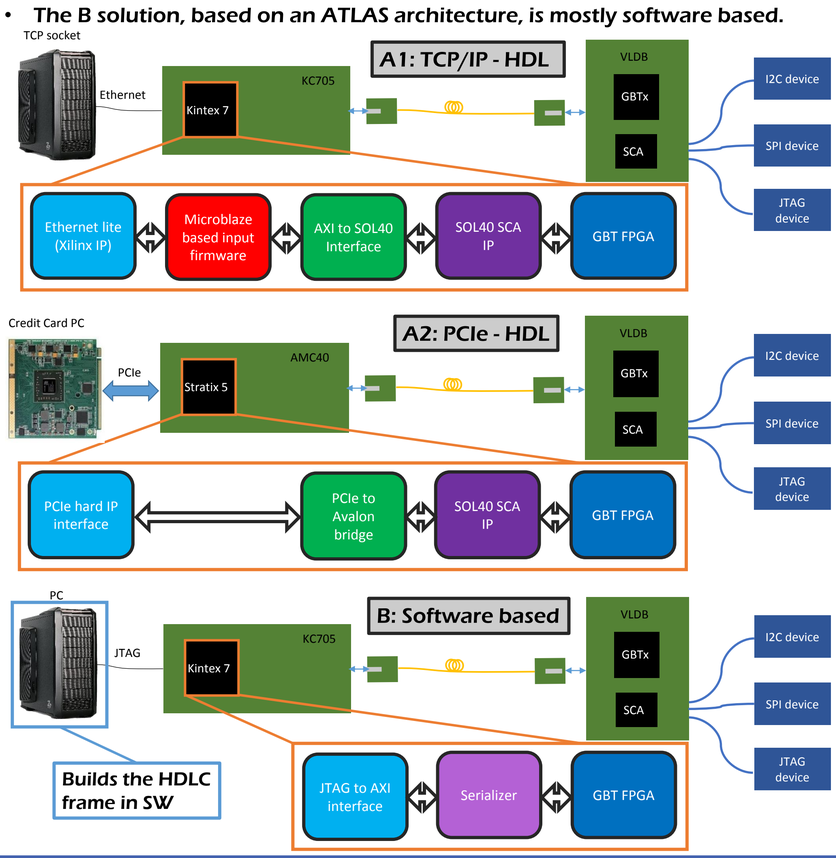


Slow Control Studies

The SCA is part of the VLDB as a fundamental piece of the GBTx ecosystem. It allows the users to communicate with modules in the experiments through different interfaces. I2C, SPI and JTAG protocols are all supported. The SCA also packs 32 GPIOs, 32 ADC inputs and 4 independent DAC channels.

Three flavours of SCA control are currently being evaluated:

- The A1 and A2 solutions (depicted in the figure below) are based on an LHCb HDL core (the "SOL40 SCA" IP)
- The B solution, based on an ATLAS architecture, is mostly software based.



Both A1 and A2 systems use the SOL40 SCA IP, which is preparing the 2 bit EC field transmitted by the GBT-FPGA core. This core provides a way to control with high parallelism and flexibility many FE chips via the GBT-SCA interfaces through GBT links. Designed as an Avalon slave, it builds and encodes/decodes GBT-SCA compliant packets, serializes and de-serializes command packets in the command word sent to the FE electronics according to GBT-SCA specifications (all the GBT-SCA protocols/channels are supported: SPI, I2C, JTAG, GPIO and ADC+DAC) and can control many GBT-SCAs per GBT link and many GBT links per FPGA. However, cascading TCP/IP and the SOL40-SCA protocols is heavy and it considerably slows down the time required to access the end-slaves (2.5s are needed to read a single I2C register in the end-device). Shorter access time are reached using the PCIe solution which is better tailored for this type of application (only 50ms for the same command). (see below the number of commands necessary to handle this single I2C read with TCP/IP).

Number of cmds for one read	TCP/IP	SOL40	SCA
I2C	27	9	1
SPI	36	12	1
GPIO	18	6	1

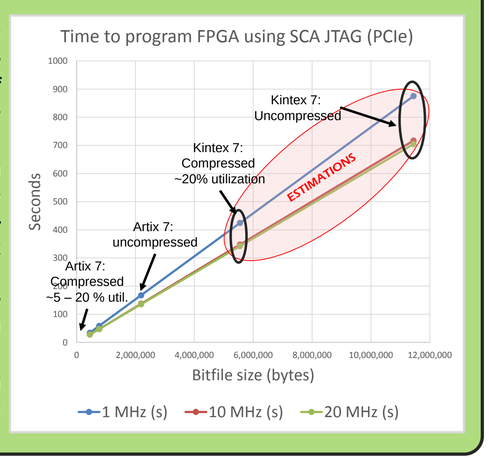
Time to read one register	I2C (400 KHz)	SPI (20 MHz)	GPIO
Including TCP/IP	2.54 s	2.71 s	1.32 s
Only SOL40 and below	214.8 µs	4.05 µs	4.05 µs

A2 setup was used to program an Artix 7 XC7A35T device over JTAG via the SCA. Unlike A1 which uses a TCP socket to control the setup from a PC, A2 uses PCI express for the same purpose.

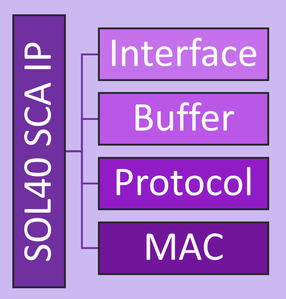
As previously mentioned, this makes a notable difference in the time required to do thousands of operations, as it is the case to program an FPGA.

The SOL40 SCA IP requires several commands to fill the 128 bit FIFO feeding the JTAG bus in the GBT-SCA. The frequency of the JTAG link only takes effect up to 10 MHz, where the overhead imposed by the SCA architecture acts as a bottleneck.

The figure shows the time needed to program 2 types of Xilinx FPGAs (Artix7 and Kintex7) using A2.



The SOL40 SCA IP is divided in 4 layers, each of them having a different function:



Interface layer: Implements a set of control and data registers.

Buffer layer: Buffer for the command to be sent to the SCA, and a memory to store one reply per channel.

Protocol layer: Transforms the data in the registers to the specific control structure of each protocol.

MAC layer: Encapsulates the data in the HDLC frame.

The SOL40 SCA IP resource usage in A1 and A2 systems is compared to the alternative B approach. In B scheme most of the processing is done in software, while the FPGA firmware basically serializes the data, passing it to the GBT FPGA.

In the following table are presented the percentage of the different FPGA resources used in a XC7K325T FPGA by the A1 system (detailing the SOL40 SCA IP, its layers and the GBT-FPGA) and by the B option (basically made of a simple serializer for EC field and the GBT-FPGA).

Module	Slice LUTs (%)	Slice Regs. (%)	Muxes (%)	Slices (%)	Block RAM Tile (%)
A1 scheme	18	9	2	33	13
SOL40 SCA IP	3.12	1.81	0.77	9.64	0.66
Interface	0.21	0.07	0.00	0.41	0.00
Buffer	2.19	1.41	0.74	8.71	0.66
Protocol	0.49	0.22	0.02	1.07	0.00
MAC	0.23	0.11	0.00	0.42	0.00
GBT FPGA	0.95	0.28	0.02	1.35	0.00
B scheme	5.24	4.03	0.83	5.27	3.19
EC serializer	0.26	0.38	0.00	0.39	0.00
GBT FPGA	0.95	0.28	0.02	1.35	0.00

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