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The Versatile Link Demonstrator Board (VLDB)

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The Versatile Link Demonstrator Board (VLDB) is the evaluation kit for the Radiation Hard Optical Link ecosystem, which provides a 4.8 Gbps data transfer link for communication between front-end (FE) and back-end (BE) of the experiments. It gathers the Versatile Link main radiation hard custom ASICs: GBTx, GBT-SCA and VTRx/VTTx plus the FeastMP, a radiation hard in-house designed DCDC.

This board is the first design allowing system-level tests of the Link with a complete interconnection of the constitutive components, allowing DAQ, control and monitoring of FE devices with the GBTx –SCA pair.

Summary

The Versatile Link Demonstrator Board (VLDB) is the evaluation kit for the Radiation Hard Optical Link ecosystem, which provides a 4.8 Gbps data transfer link for communication between front-end (FE) and back-end (BE) of the experiments. It gathers the Versatile Link main radiation hard custom ASICs: GBTx (ASIC dedicated to serialization, deserialization and data and clock recovery), GBT-SCA (Slow Control Adaptor ASIC dedicated to FE control and status monitoring) and VTRx/VTTx (optical transceiver/dual transmitter) plus the FeastMP, a radiation hard DCDC designed at CERN. It manages timing signal, trigger, status monitoring, readout data and slow control of FE devices.

Already distributed to 40 teams, this board is the first design allowing system-level tests of the Versatile Link with a complete interconnection of the constitutive components. HDMI connectors allow to test communication with experiments Front-End electronics (up to 20 Front End ASICs can be connected via elink/HDMI to the same GBTx). They also allow to try multiple interconnection schemes between several VLDBs playing all the roles foreseen by the various use cases or to focus on slow control using the GBT-SCA chip. It is a unique tool for initial characterization of the full Radiation Hard Optical Link ecosystem (in particular focussing on the quality of recovered clock delivered to the Front-End electronics, latency of delivered triggers or data link characterization). It is also the ideal guinea-pig to test software and firmware implementation at Back-End level and to control complex systems based on multi-GBT implementations. It can also be used for preliminary on-site system tests. Finally, it is an excellent reference for future board designs using these components.

The VLDB board will be presented as well as several interconnection schemes emulating experimental setups. A demonstrator implementing slow control of various Front-end devices over GBTx and GBT-SCA will be described. Finally, the results of various characterization campaigns of the GBTx and on the full link -based on the VLDB- will be commented, such as clock stability with varying temperature, radiation tests and latency tests.

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