PROTOTYPE READOUT ELECTRONICS FOR THE UPGRADED ALICE INNER TRACKING SYSTEM

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INTRODUCTION

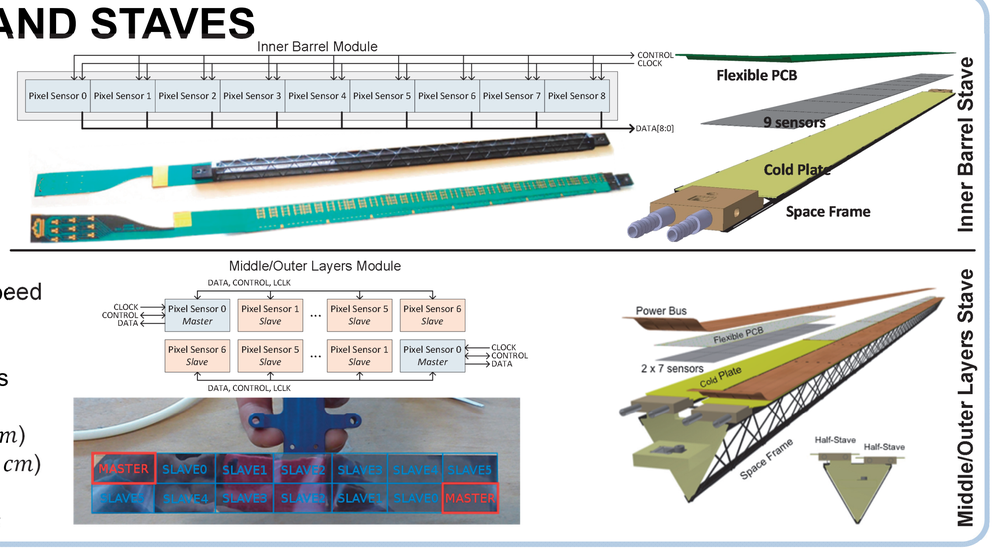
ALICE (A Large Ion Collider Experiment) is an experiment designed to study the properties of the Quark-Gluon Plasma (QGP) using proton-proton, proton-nucleus and nucleus-nucleus collisions at the CERN Large Hadron Collider.
The ALICE Collaboration is preparing **a major upgrade** of the experimental apparatus, planned for installation in the second LHC shutdown in the years 2018-2020. A key element of the ALICE upgrade is the construction of **a new, ultra-light, high-resolution, 7-layers Inner Tracking System (ITS)** [1]. Its main functions are tracking charged particles in a magnetic field for momentum measurements and the reconstruction of the primary and secondary interaction vertices. The ITS is the most innermost barrel detector of the ALICE apparatus surrounding the interaction point.

PIXEL SENSORS, MODULES AND STAVES

Pixel sensor:
- $0.18\ \mu m$ CMOS Monolithic Active Pixel Sensor
- $30\ mm \times 15\ mm$, thinned down to $50\ \mu m$
- low power
- high-speed digital, differential output interface

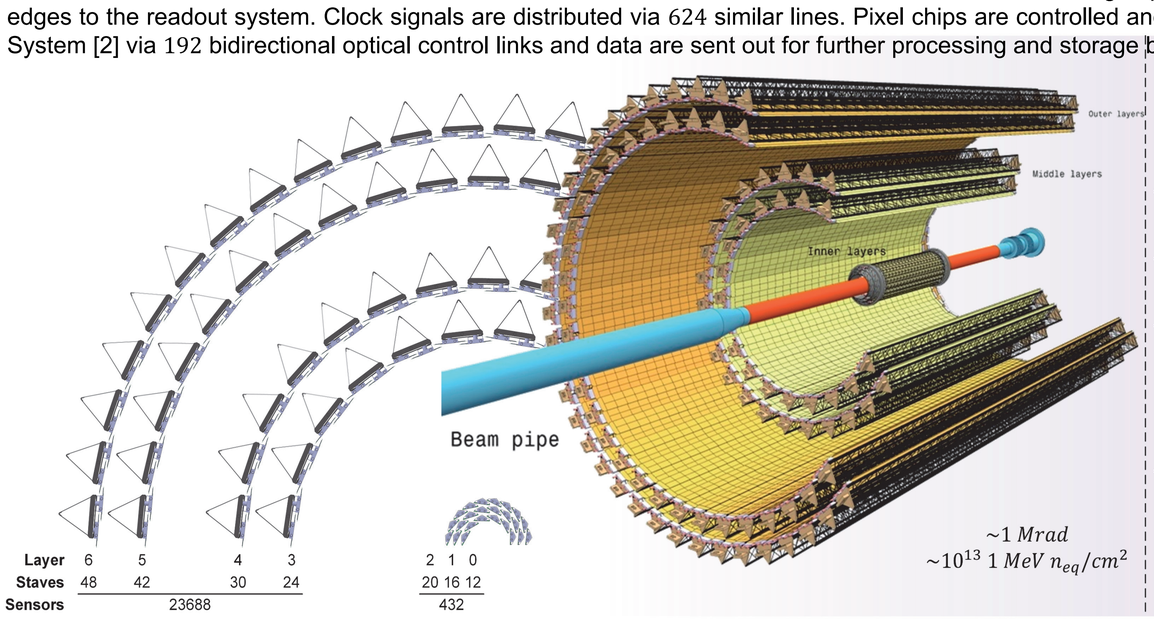
Inner Barrel module:
- 9 pixel chips per module (physical length $30\ cm$)
- shared clock and control signals, 9 independent high-speed output data lines running at $1.2\ Gbps$

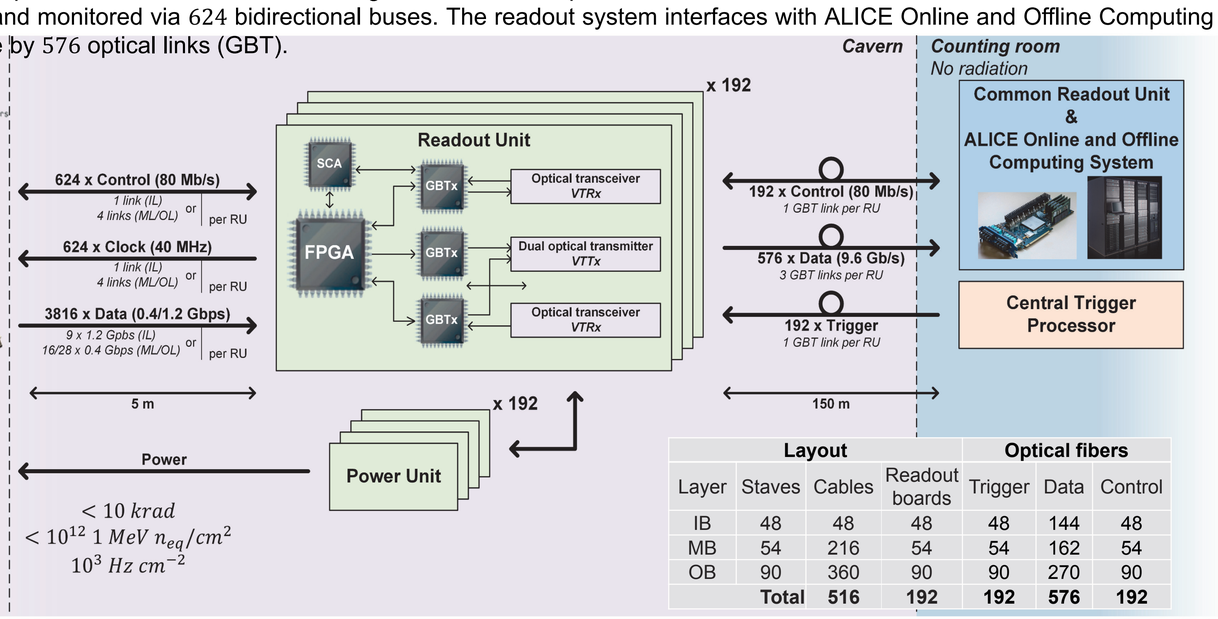
Middle and Outer Barrel modules:
- each stave is made up of modules (one module consists of 7 pixel chips in 2 rows with one master chip per row)
- 8 modules per Middle Layer Stave (physical length $80\ cm$)
- 14 modules per Outer Layer Stave (physical length $150\ cm$)
- clock and control signals shared by modules, 16 or 28 independent data outputs running at $400\ Mbps$



READOUT SYSTEM ACHITECTURE

The ITS Readout System is composed of 192 electronic boards (Readout Units) located $5\ m$ from the detector. They configure and control the pixel chips, receive and assemble data and manage power units. Each Readout Unit and Power Unit are connected to one detector's stave. The data are read out via 3816 differential high-speed lines. These are made of segments of microstrip lines on the FPCs and of micro-twinax cables from the FPC edges to the readout system. Clock signals are distributed via 624 similar lines. Pixel chips are controlled and monitored via 624 bidirectional buses. The readout system interfaces with ALICE Online and Offline Computing System [2] via 192 bidirectional optical control links and data are sent out for further processing and storage by 576 optical links (GBT).





Layout				Optical fibers		
Layer	Staves	Cables	Readout boards	Trigger	Data	Control
IB	48	48	48	48	144	48
MB	54	216	54	54	162	54
OB	90	360	90	90	270	90
	Total	**516**	**192**	**192**	**576**	**192**

THE ITS PROTOTYPE READOUT UNIT

The Prototype Readout Unit (ITS_RUv0a) was designed to address many different R&D activities regarding the ITS Readout System development. The basic prototyping platform has been used by many scientists at CERN and in the USA, the Netherlands and the Czech Republic for almost one year. Due to its versatile architecture, it allows for testing and verification of the interface between sensor modules and readout electronics, signal integrity and data transfer reliability over $5\ m$ long twinax cables, the interface to the power units and to the ALICE O^2 Computing System and the triggering capabilities. It is also utilized during beam tests where the FPGA's operation is evaluated and methods for mitigating radiation effects are developed and characterized.

The Prototype Readout Unit is the basic prototyping platform that has been used to develop the Readout System for the Upgraded ALICE Inner Tracking System for almost one year.

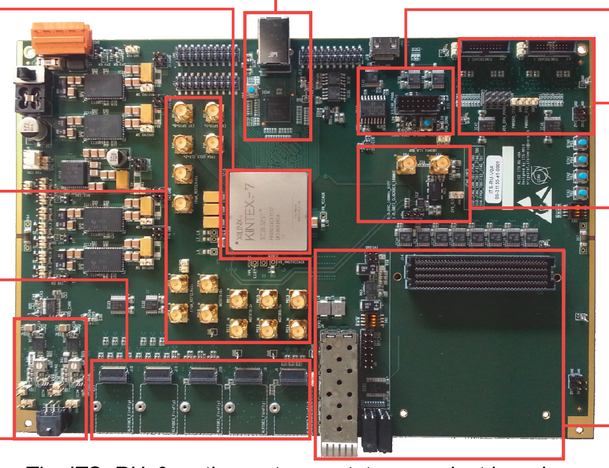
Xilinx Kintex-7 325T is utilized to receive data from the pixel sensor, to send it out for further processing and to evaluate its operation in the radiation environment

Unconnected transceivers and clock inputs can be accessed from outside to enable more flexibility while developing firmware

Many termination topologies enable studying different connection schemes with the IL/ML/OL modules

Controllable power supply powers the chip module and monitors its power consumption

The Cypress FX3 controller provides USB 3.0 communication with a PC



The ITS_RUv0a – the custom prototype readout board with Xilinx Kintex-7 XC7K325T-2FFG900 FPGA

FPGA can be configured using JTAG, Flash memory or GBT-SCA to enable many different R&D activities (normal operation, FPGA scrubbing etc.)

Connection to the ITS Power Unit is added to test communication with it and operability

To provide a versatile clocking scheme the Prototype Readout Unit can operate using a local $160\ MHz$ clock, a machine $40\ Mhz$ clock received from the GBTx chip and a clock received from outside

Communication between GBTx and GBTx-FMC board [5] inserted to the FMC slot and an optical SFP module

RADIATION SUSCEPTIBILITY TESTING

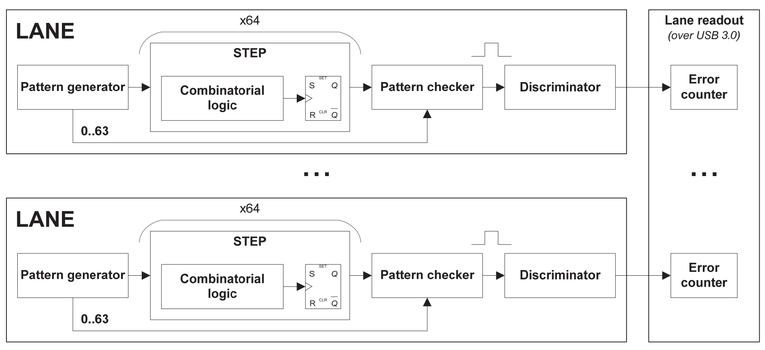
The prototype readout unit was used as a platform for radiation susceptibility testing. Both the Xilinx Kintex-7 325T FPGA and the GBTx chip were irradiated. The irradiation experiments were conducted at the isochronous cyclotron [3] located at the Nuclear Physics Institute of the Academy of Sciences of the Czech Republic in Řež near Prague. The machine provides a proton beam with an energy range from 6 to $37\ MeV$. The equivalent proton flux ranges from 10^4 to $10^{14}\ cm^{-2} \cdot s^{-1}$, over a uniform area of about $2.5 \times 2.5\ cm^2$.

During the irradiation campaign:
- FPGA's CRAM cross-section was measured to be $4.02 \cdot 10^{-15}\ cm^2 \cdot bit^{-1}$
- Operation of the Xilinx Soft Error Mitigation IP (SEM IP) was investigated
- Mitigation techniques of radiation effects were studied and characterized

Before applying the mitigation technique, the structure to be protected must be studied to find the most appropriate method to implement.

The logic testing firmware consists of test structures called lanes. In each lane there is a pattern generator, a logic test structure, a pattern checker and a discriminator. The pattern generator generates 6-bit test vectors (from 0 to 63). The logic test structure (STEP) is replicated 64 times, forming an array that shifts the test vectors. It is built from an LUT hard-coded transfer function (combinatorial logic) and an output register. It is possible to multiplicate either the combinatorial logic, output register or both. Depending on the selected multiplication level, the firmware was compiled with 256, 160, 128 or 64 lanes. The pattern checker compares the output from the array of logic test structures with the output from the pattern generator. If a discrepancy is found, an error pulse is generated and an error counter is incremented. The values stored in the error counters are read out over the USB 3.0 interface for further analysis.

Results obtained in the beam test and the fault injection test are comparable. If a voter's physical cross-section is higher than the cross-section of the protected circuit, then a decrease of radiation susceptibility can be observed. Triplication of the combinatorial logic circuit lowers down the test structure's cross-section at the expense of utilization of larger amount of device resources.



A diagram of the logic testing firmware

	Fluence $\left[\frac{p}{cm^2}\right]$	Lanes	Faulty lanes: Mean	Faulty lanes: Std. dev.	STEP cross-section $\sigma\ \left[\frac{cm^2}{STEP}\right]$	Error $\delta\sigma\ \left[\frac{cm^2}{STEP}\right]$
Fault injection test						
Nothing triplicated	$0.74 \cdot 10^7$	256	19.96	4.33	$13.0 \cdot 10^{-13}$	$3.36 \cdot 10^{-14}$
STEP output registers triplicated	$0.74 \cdot 10^7$	160	17.64	5.42	$19.6 \cdot 10^{-13}$	$6.38 \cdot 10^{-14}$
Combinatorial logic triplicated	$0.74 \cdot 10^7$	128	5.46	2.28	$7.11 \cdot 10^{-13}$	$3.30 \cdot 10^{-14}$
Both triplicated	$0.74 \cdot 10^7$	64	1.71	1.18	$6.75 \cdot 10^{-13}$	$3.34 \cdot 10^{-14}$
Beam test						
Nothing triplicated	$0.74 \cdot 10^7$	256	12.71	3.76	$8.74 \cdot 10^{-13}$	$3.28 \cdot 10^{-14}$
STEP output registers triplicated	$0.74 \cdot 10^7$	160	11.74	3.13	$12.9 \cdot 10^{-13}$	$4.73 \cdot 10^{-14}$
Combinatorial logic triplicated	$0.74 \cdot 10^7$	128	2.63	1.83	$3.62 \cdot 10^{-13}$	$3.48 \cdot 10^{-14}$
Both triplicated	$0.74 \cdot 10^7$	64	1.07	1.00	$2.94 \cdot 10^{-13}$	$4.14 \cdot 10^{-14}$

Comparison of the cross-sections obtained from the beam test and the fault injection test

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