A UNIVERSAL FMC BASED DAQ SYSTEM FOR DETECTOR APPLICATIONS

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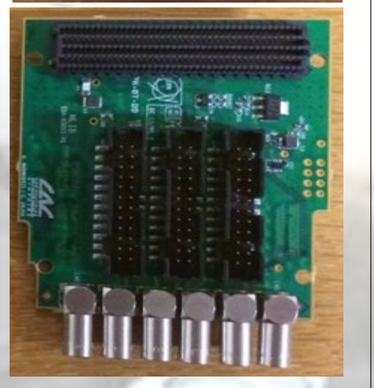
Concept and Requirements

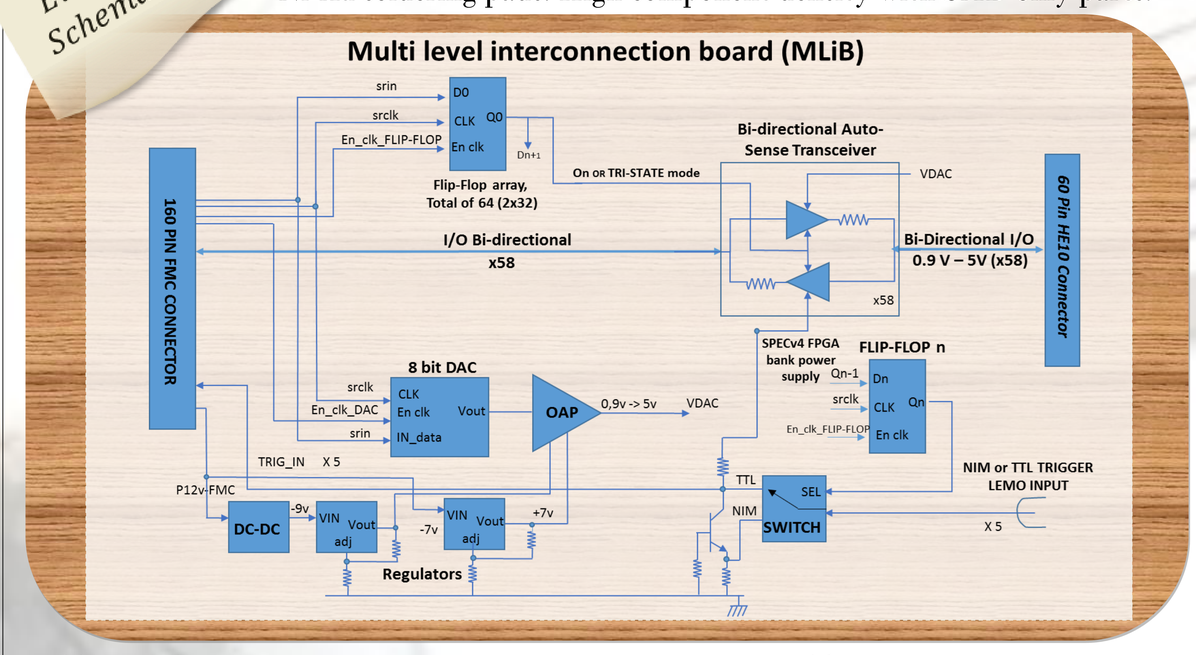
- → **Detector DAQ system providing compatibility with different ASICs technology**
- → **Open architecture**
- → **Commercial availability of components**
- → **Low cost**
- → **Operation at HL-LHC conditions (40 MHz rate)**
- → **Compact design and ease of use with single unit integration**
- → **Upgradability and array testing possibility**



Design and production

Versatile off-the-self commercial components used with low cost and increased availability. Design optimized for noise reduction in the digital channels with an 8 layer board using 35 μm cooper corridors and Ni-Au soldering pads. High component density with SMD only parts.

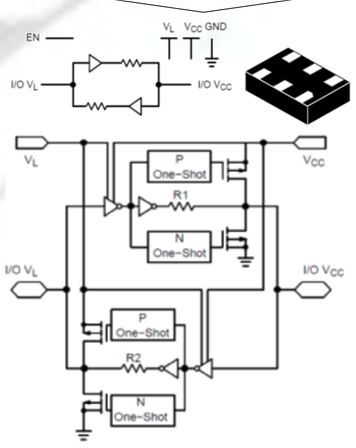
Electrical Schematics



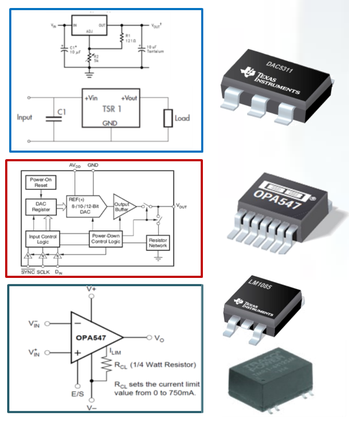
Implementation—characteristics

Based on the SPEC PCIe card providing a 4Gbit interface, equipped with a Xilinx Spartan 6 FPGA and FMC interface. 68 digital outputs available at 2.5 V and 12V powering for daughter board.

Adjustable multi-level transceivers form 0.9V to 4.8V with automatic bi-directionality and programmable high-Z functionality to isolate individual channels. Rated up to 80MHz,



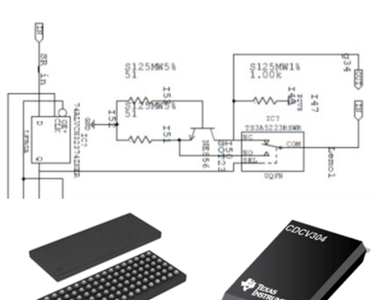
Embedded 8bit DAC for continuous output signal level adjustment and integrated symmetric amplifier to drive all 64 available channels. On board power supply to avoid need for external powering.



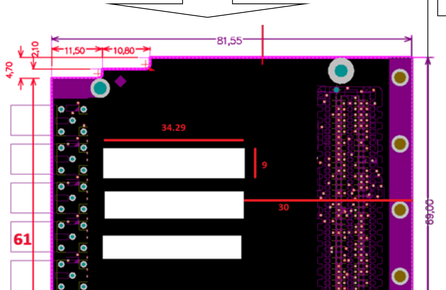
Design Specificaitons			
Available Channels	64 independently operated	**DAC**	8bit programmable
Signal level	0.9 V - 4.9 V	**Output protection**	Zener on every I/O
Input level	2.5 V	**Power voltage**	12 V internal
Signal type	Direct or pseudo-differential	**Trigger inputs**	6 (TTL/NIM)

FMC socket use makes system transposable to any platform. Trigger inputs are implemented with LEMO connectors while signal output with standard HE-10 low density connectors for compatibility.

Six programmable NIM/TTL trigger inputs implemented. Serial programming for DAC, trigger and all 62 channels with 2 independent clocks sacrifices only two FPGA inputs.



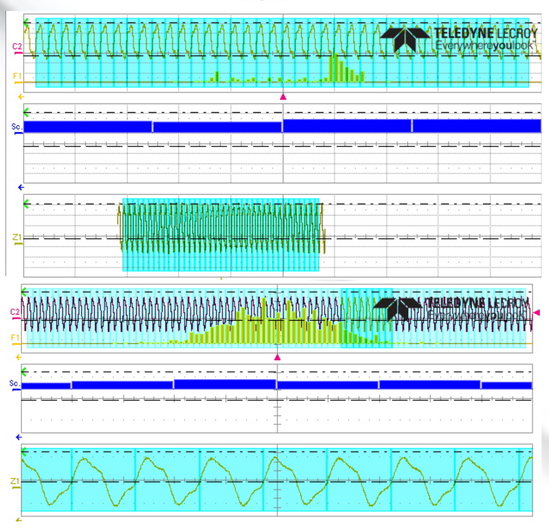
Card maintained within standard FMC footprint with trigger connectors placed on front panel for easy access. Signal inputs placed on backside and aligned with openings on mother-board.



Characterization and testing

Measurements performed on prototypes demonstrated a rise-time estimate of 5 nsec at 20MHz. Noise levels where measured at 10—40 MHz found to be in the order of 30 mV for direct 1.3 V signals using a 1 m ling cable at a non-shielded configuration,

Rise time analysis at 40MHz demonstrated an estimated variation from 5 to 9 nsec. This allows safe operation within the 25 nsec period. Jitter estimations where performed at 20 MHz were a 56 psec value was determined.



N in P, VTT production, <100> orientation	
Noise	30mV at 10—20 MHz
Rise Time	5 nsec at 20 MHz, 9 nsec at 40MHz
Jitter	56 psec

Sensor Read-out study

Front-end card featuring an Omegapix assembly, including the 3D implemented ASIC bump-bonded to an ADVACAM 150 μm sensor and read out by the MLIB system. Different front-end cards are available, each adapted to the specific ASIC application.

An FPGA firmware module allowing to control the card was created and in addition with LabView interface data were acquired for the Omegapix ASIC. A cumulative noise distribution of a bonded ASIC with a sensor is presented with respect to the pixel map.