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## A Universal FMC-Based DAQ System

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Towards development of a 10MGy rad-hard ASIC, evaluation of innovative 3D integration technology and CMOS - active edge pixel sensor characterization, a versatile DAQ system is presented. Based on a Saprtan 6 PCIe board, an FMC mezzanine card is developed providing a 68-channel digital input. Featuring automatic bi-directionality and variable output level (0.9V - 4.8V) with high impedance capability, each channel is independently adjustable. The 8.5ns transceiver rise time assures required 40MHz rate for HL-LHC conditions. An 8bit ADC combined with clock buffering and serialization, limit to four the number of control lines.

### Summary

Towards the development of a 10MGy radiation hard pixel ASIC, the evaluation of the innovative 3D integration technology and advances in CMOS and active edge planar pixel sensors, a versatile and universal data acquisition system is needed, compatible with different technologies. With availability, simplicity and low-cost as primary requirements, an FPGA-based DAQ system is developed based on a CERN developed FMC PCIe 2.0 carrier board. Base board provides a total of 34 differential or 68 direct line inputs hard-wired at 2.5V signal level.

A specially conceived FMC mezzanine card is developed, providing a programmable 58 digital channel input. Featuring automatic embedded bi-directionality and variable signal level from 0.9V to 4.8V with high impedance capability, each channel is independently adjustable. Use of an 8bit analog to digital converter allows for a quasi-continuous output signal level stepping. The 8.5ns transceiver rise time assures the required 40MHz input rate expected in HL-LHC conditions while, a fast on the fly channel independent switching is provided.

To minimize the number of needed control lines, clock distribution, buffering and serialized programming are exploited. In addition, six integrated trigger inputs are instrumented, compatible with both TTL and NIM standards via firmware control. A low noise amplifier and embedded switching power supply eliminate the need for external powering, restraining the system to standard FMC specifications in both footprint and powering requirements. Power dissipation studies at full load confirm a low thermal budget on the support structure with no need for external cooling components.

The FPGA firmware control module was conceived for fast integration with application-specific firmware, allowing direct communication and interaction with LabVIEW™ based or autonomous UNIX compiled data acquisition software. The system is provided as a full package with proven functionality as a silicon detector ASIC read-out while, its versatility allows for use in a variety of R&D projects.

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