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ATLAS Phase-II-Upgrade Pixel Data Transmission Development

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The ATLAS tracking system will be replaced by an all-silicon detector (ITk) in the course of the planned HL-LHC accelerator upgrade around 2025. The readout of the ITk pixel system will be most challenging in terms of data rate and readout speed. Simulation of the on-detector electronics based on the currently foreseen trigger rate of 1 MHz indicate that a readout speed of up to 5 Gbps per data link is necessary. Due to radiation levels, the first part of transmission has to be implemented electrically. System simulation and test results of cable candidates will be presented.

Summary

ATLAS is preparing for an extensive modification of its detector in the course of the planned HL- LHC accelerator upgrade around 2025 which includes a replacement of the entire tracking system by an all-silicon detector (Inner Tracker, ITk) and a revised trigger and data taking system with triggers expected at lowest level at an average rate of 1 MHz. The five innermost layers of ITk will comprise of a pixel detector. The readout of the pixel layers will be most challenging in terms of data rate and readout speed. A new on-detector readout chip is designed in the context of the RD53 collaboration. The performance of the readout system was simulated based on hit rates from detector simulation combined with behaviour expected from the proposed chip design, assuming different buffer sizes to store data until trigger arrival with proposed trigger parameters. This simulation indicates that a readout speed of up to 5 Gb/s per data link is necessary in the innermost layers going down to 640 Mb/s for the outermost layers while adding a latency well below that imposed by the ATLAS trigger system. Up- and downlink communication to the on-detector electronics is foreseen to be largely optical. However, radiation levels close to the beam pipe prevent the placement of optical components close to the readout chips such that the first part of transmission has to be implemented electrically with signals to be converted for optical transmission at larger radii. Options to group data links of outer layers are considered in order to make use of the bandwidth to be made available for innermost layers and thus reduce needed material. Consequently, cables are being developed for electrical data transmission at rates of up to 5 Gb/s over several metres. Designs cover solutions such as twin-axial, twisted pair or flex cables and hybrids of these. Prototype cable performance was inspected with dedicated bit error rate testers based on FPGA boards or commercial types. Error rate measurements are complemented by attenuation behaviour derived from S-parameter analysis and eye-diagram inspection in addition to according simulations. Some of the cables under test demonstrated maximum payload rates above the desired data rate and thus provide good candidates for the ITk-Pixel readout.

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