# ALICE ITS READOUT ELECTRONICS PROTOTYPE TESTING WITH THE CERN GBT TRANSCEIVER

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*On behalf of the ALICE Collaboration*

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## INTRODUCTION

The ALICE experiment is studying strongly interacting hadronic matter using nucleus-nucleus, proton-nucleus, and proton-proton collisions at the CERN LHC. To deal with the increased interaction rates expected for Run-3, the ALICE detector will be upgraded during the LHC shutdown 2019/20. The upgrades include a new, **high-resolution, low-material Inner Tracking System (ITS)** based on Monolithic Active Pixel Sensors (MAPS) developed by the ITS collaboration [1]. A total of ~25k sensors are distributed in 7 concentric barrels (at radii from 22 to 400 mm), sub-divided into staves (30 – 150 cm length) and provide a detection area of 10 m$^2$ segmented into more than 12.5 G Pixels. The new ITS will improve the impact parameter resolution, provide better tracking efficiency and $p_T$ resolution and acceptance at low $p_T$, and allow for fast insertion and removal.

## SENSOR, MODULE & STAVE

**Pixel sensor:**

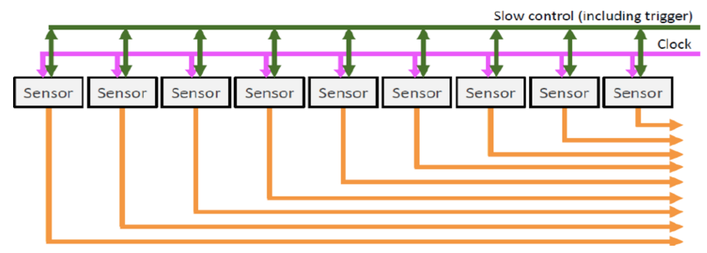
- $0.18\ \mu m$ CMOS Monolithic Active Pixel Sensor
- size: $30x15\ mm^2$, thinned down to $50\ \mu m$ (IB) or $100\ \mu m$ (OB)
- low power
- high-speed digital, differential output interface

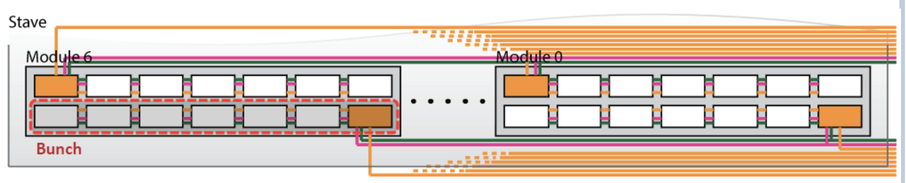
**Inner Barrel staves:**

- 9 pixel sensors per stave (physical length $30\ cm$)
- shared clock and control signals
- 9 independent high-speed output data lines running at $1.2\ Gbps$

**Middle (and Outer) Barrel staves:**

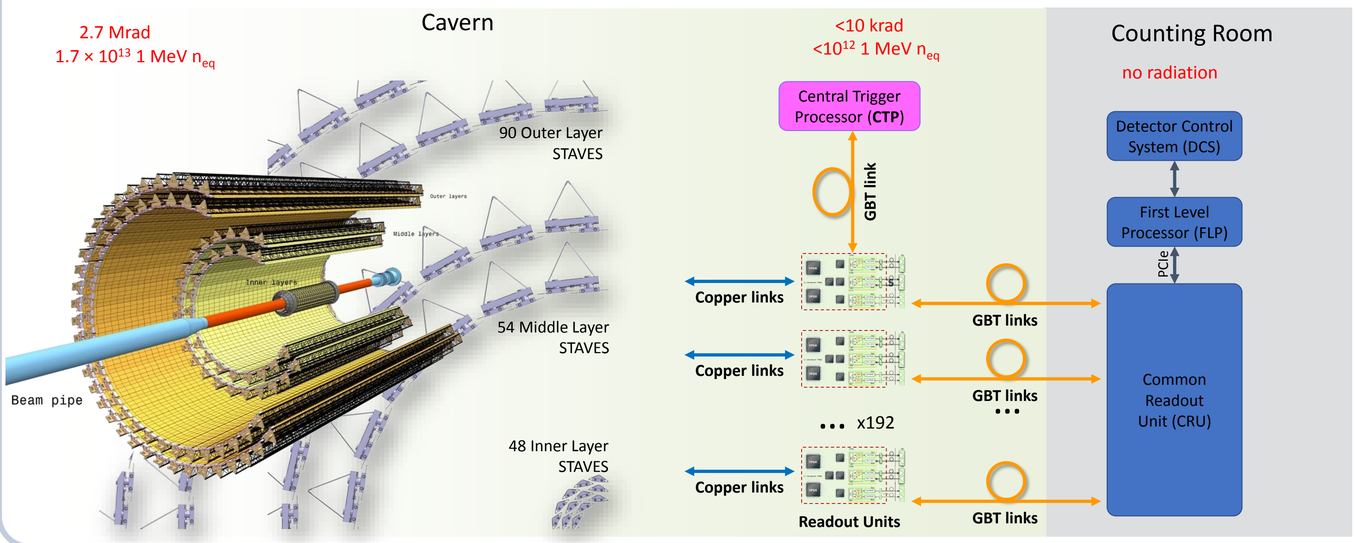
- each stave is made up of two rows of 4 (7) "modules"
- each module consists of two rows of 7 sensors with 1 master and 6 slave sensors each on a flex printed circuit board
- clock and control signals shared on module by each row
- 16 (28) independent data outputs running at $400\ Mbps$



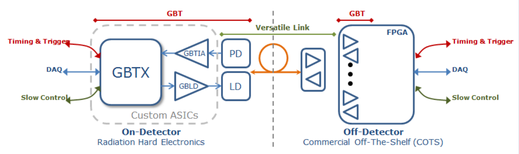

## ITS upgrade READOUT SYSTEM ACHITECTURE

The ITS upgrade requires a new readout system designed to read the ITS data up to a rate of 100 kHz (400 kHz) for Pb-Pb (pp) collisions. The readout system connects to the sensors using differential copper links for the data, control and clock signals, receives trigger signals from the central trigger processor and control/configuration data from the counting room, and delivers sensor data to the counting room using (bi-directional) optical fibers. The current design for this readout system foresees a modular Readout Unit (RU), each connected to one stave, resulting in a total of 192 RU's. The RU's will be located 5 m from the end of the staves in the experimental hall. This location is characterized by a radiation environment resulting in a total ionizing dose of <10 krad and a high-energy hadron flux (capable of causing single-event upsets in the RU's) of ≈ 1 kHz·cm$^{-2}$. The RU design consists of an FPGA to deal with control of the sensors, handling the trigger and data collection, formatting, forwarding using the "**Gigabit Transceiver Optical Link" (GBT).** The GBT, developed at CERN for the LHC experiment upgrades [2], consists of the GBTx serializer/deserializer ASIC, the VTRx/VTTx optical transceiver/transmitter module, and the GBT-SCA slow control ASIC.




| Layer | Staves | Cables | Readout boards | Trigger | Data | Control |
|---|---|---|---|---|---|---|
| | Layout | | | Optical fibers | | |
| IB | 48 | 48 | 48 | 48 | 144 | 48 |
| MB | 54 | 216 | 54 | 54 | 162 | 54 |
| OB | 90 | 360 | 90 | 90 | 270 | 90 |
| | **Total** | **624** | **192** | **192** | **576** | **192** |

"Gigabit Transceiver" (GBT)



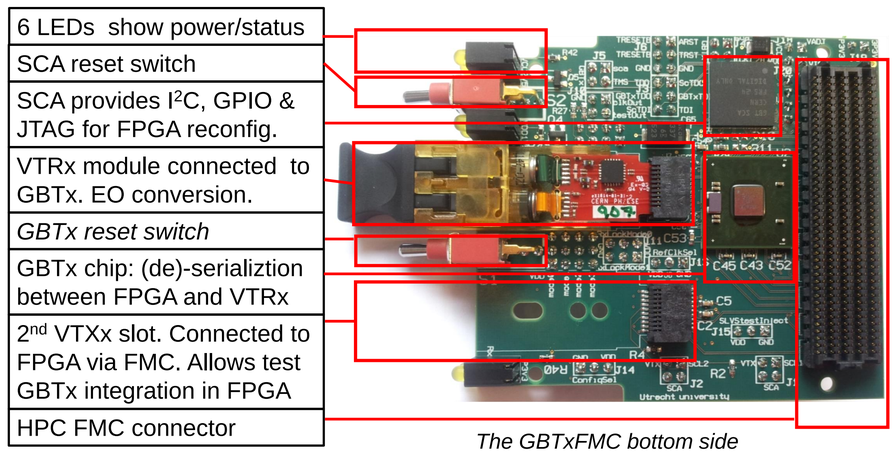

## RU prototype and GBTxFMC

A RU prototype [3] was developed to allow firmware development and interface (sensor, DAQ, CTP, Power Unit) and radiation testing. Placing the components for the GBT link on a seperate FMC [4] module ("GBTxFMC") provided the following advantages:

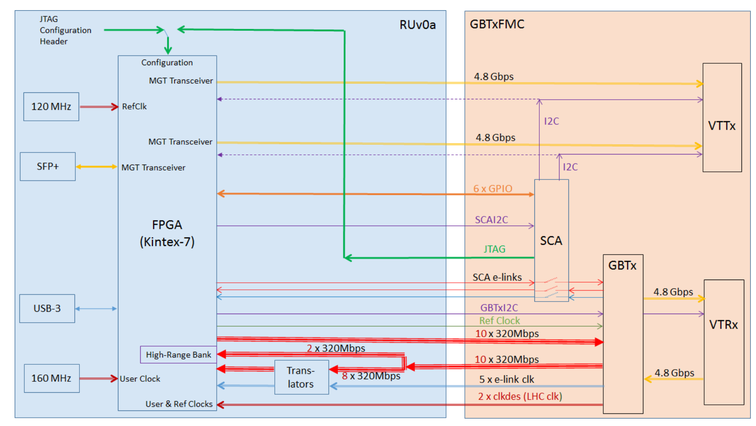
- Concurrent development: RU at CERN, GBTxFMC at UU/Nikhef
- A GBTxFMC module that can be used on other boards, development kits (e.g. SF2 and RTG4) and/or by other users

GBTxFMC features/functionalities:

**GBTX ASIC:** configurable by USB-I2C dongle via 8 pins header
**E-links:** delay matched: 25 ps within group, between max 170ps
**E-links:** All 320Mbps pairs are available on the LPC pins.
**GBT-SCA ASIC:** resistors allow e-links to bypass SCA
**VTRx/VTTx:** Laser driver diode power controlled by I2C



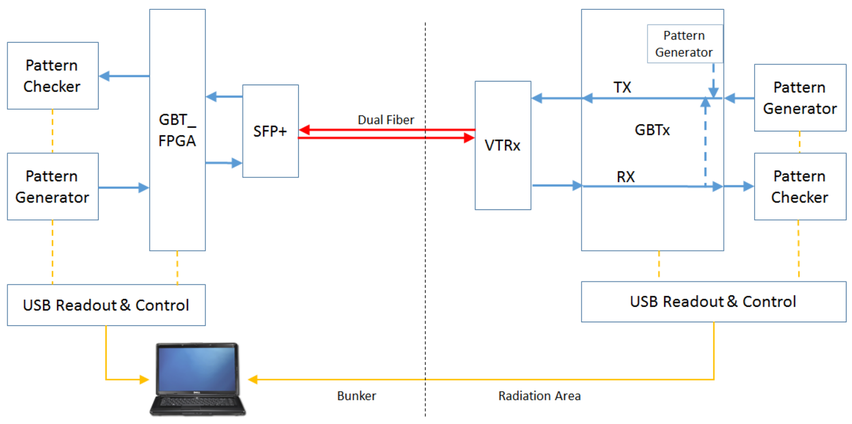

*The GBTxFMC bottom side*



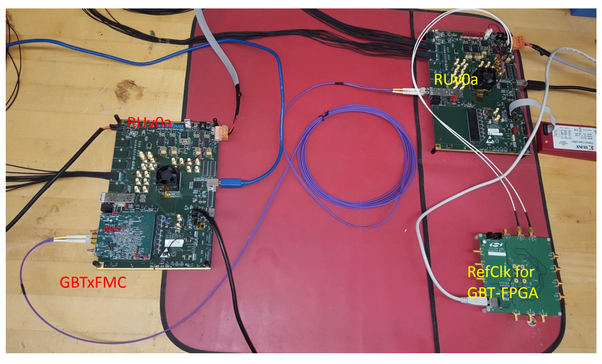

*GBTxFMC connected to the ITS Readout Unit Prototype Board "RUv0a"*

## GBT Testing

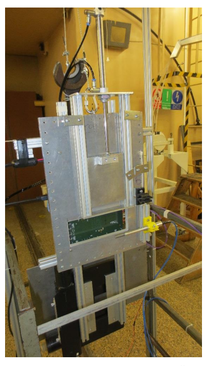
The combination of the RU prototype ("RUv0a") and the GBTxFMC allowed to test both the connections between the GBTx and FPGA as well as some of the interfaces provided by the GBT-SCA ASIC.




*Block diagram of the test setup with 2 RUv0a, one running GBT-FPGA, the other interfaced to the GBTx*




*Two board test setup at UT Austin for both lab and radiation testing*



*Radiation test setup at Řež*

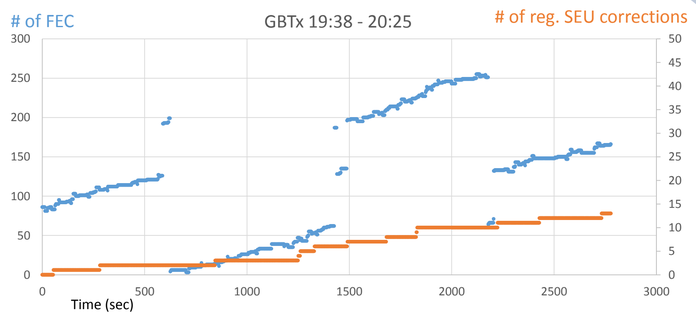
The ten 320 Mbps **e-links** of the **GBTx** were connected to the FPGA with and without level-translators. Initial tests verified that these level translators are not needed to interface with the Kintex-7 I/O's. Five e-link clocks allowed synchronization of the FPGA data with the GBTx. The RUv0a board includes an SFP+ connection to the FPGA transceiver to allow implementation of the GBT protocol in the FPGA, thus enabling the emulation of the counting house electronics in the same firmware that also controls the GBTx, or on a second RUv0a. Both the GBT-FPGA firmware and the GBTx control firmware are interfaced to a USB-3 interface on the RUv0a, which allows control and monitoring of these firmware modules from a PC. An I2C firmware module allows to configure and monitor the GBTx chip via USB. The setup with 2 RUv0a boards connected via a GBT link from **GBT-FPGA** to **GBTx** is shown in the photograph at the bottom left.

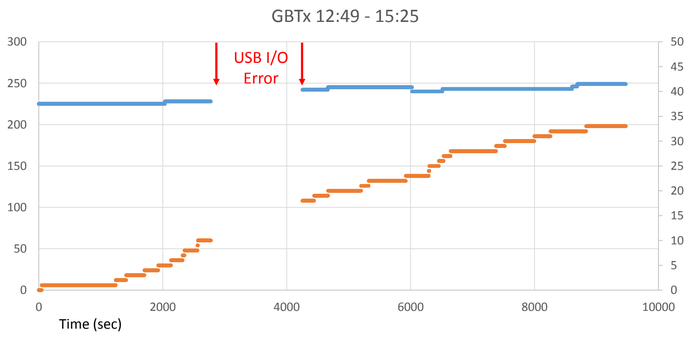
The GBT-SCA has the **JTAG**, 6 of the 32 **GPIO** pins, and **I2C** channels connected to the FPGA to provide testing of these interfaces. A firmware interface to the GBT-FPGA core was developed to control the various GBT-SCA channels through the GBT-FPGA. The GPIO interface bits were tested in both directions through the path:

***FPGA – GBT-SCA – GBTx – GBT-FPGA – USB***.

The SCA JTAG channel is connected to the configuration port of the FPGA with the intention to load FPGA firmware over the GBT link. Initial tests with a JTAG ID command to the FPGA allowed verifying this path. A simple I2C slave interface firmware in the FPGA verified this channel of the GBT-SCA.

Since the ITS readout system will be installed in a moderate radiation environment, we also designed a setup as shown in the block diagram at the top left, consisting of a pattern generator and checker interfaced to the GBT-FPGA firmware, connected to the GBTx on a second RUv0a, where a second set of pattern generator and checker is implemented in the FPGA. The pattern checkers in both FPGAs include error counters that can be read over USB. The GBTx includes configurations to allow internal pattern generators and loopback within the GBTx. The USB interface also allowed the readout of various GBTx internal monitoring registers, including the number of Forward Error Corrections (FEC) in the RX and SEU corrections in the configuration registers.




The irradiation experiments were conducted at the cyclotron [5] of the Nuclear Physics Institute of the Academy of Sciences of the Czech Republic in Řež near Prague. The machine provides a proton beam with an energy range from $6$ to $37\ MeV$. The equivalent proton flux ranges from $10^4$ to $10^{14}\ cm^{-2} \cdot s^{-1}$, over a uniform area of about $2.5 \times 2.5\ cm^2$.

The plots above show the results for the FEC counts and SEU correction counts in the GBTx, at top for the GBTx in transceiver mode, while the bottom used the GBTx TX-only mode. The flux in both cases was ~1E+8 at a proton energy of 35 MeV. Although multiple FEC counts were observed, the pattern checkers registered no bit-errors in both cases, thus verifying the effectiveness of the FEC. Comparison of the plots shows that the FEC is mostly necessary for the RX case in radiation.

## REFERENCES

[1] The ALICE Collaboration. Technical Design Report for the Upgrade of the ALICE Inner Tracking System. In J.Phys. G41 (2014) 087002 [CERN-LHCC-2013-024. ALICE-TDR-017].
[2] GBT project home page: https://espace.cern.ch/GBT-Project/default.aspx
[3] K. M. Sielewicz et al, prototype readout electronics for the ALICE inner tracking system upgrade, TWEPP2016
[4] FMC, FPGA Mezzanine Card, ANSI/VITA 57.1 standard, http://www.vita.com/fmc
[5] NPI Řež, Department of Accelerators, "Web Site." [Online]. Available: http://accs.ujf.cas.cz/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