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## Phase 1 Upgrade of the CMS Drift Tubes Read-Out System

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In order to cope with a twofold increase in nominal LHC luminosity, the second level of the readout system of the CMS Drift Tubes (DT) electronics needs to be redesigned to minimize event processing time and remove present bottlenecks. The uROS boards are uTCA modules, which include a Xilinx Virtex-7 FPGA and equip up to 6 12-channel optical receivers of the 240 Mbps input links. Each board collects the information from up to 72 input links (3 DT sectors), requiring a total of 23 boards. The design of the system and the first validation tests will be described.

### Summary

The readout system of the Muon Drift Tubes (DT) subdetector of the CMS (Compact Muon Solenoid) experiment is organized in several levels. The Readout Board (ROB), located on the detector itself, constitutes the first stage, performing time-to-digital conversion (TDC) of the pulse edges from 128 DTs, storage, and window matching when the level-1 accept (L1A) trigger signal is received. The second level, so-called Readout Server (ROS), is in charge of receiving data from 25 ROB, performing data integrity verifications, building synchronized event blocks and merging the information into higher-bandwidth links to the next level of the readout chain. The ROS was located in the harsh environment of the experimental cavern, and was relocated to the service cavern during the 2013-2014 long shutdown to ease subsequent upgrades.

Simulations show that the ROS processing time is the current most severe bottleneck in the readout chain, and it will not be able to deliver the necessary performance to cope with the expected twofold increase in luminosity for the LHC in the coming years

A common uTCA-based design was developed for the DT trigger (TwinMux) and readout (uROS) second-level electronics upgrade, implementing different firmware. The uROS is a single-slot double-width and full-height Advanced Mezzanine Card (AMC) based around a Xilinx Virtex-7 FPGA that includes optic transceivers for slow-speed inputs and high-speed output data transmission up to 13 Gbps.

The DT system is divided in 5 wheels, with 12 sectors each. Each sector's data is arranged in 25 fibres, making a total of 1500 links, which will be distributed in 23 uROS boards across 3 uTCA crates. Each uROS will receive and deserialize the input data, perform data quality monitoring, and build an integrated event synchronized with the CMS Trigger, Timing and Control system to be delivered through a 5 Gbps high speed link in the uTCA backplane to the so-called AMC13 board, which subsequently transmits to the CMS Central DAQ system. The uROS also contains 24 high speed (up to 13 Gbps) optical output links in case of future DAQ upgrades. The uROS will connect to the CMS IP network through the MCH (Micro TCA Carrier Hub) for slow control and monitoring.

The uROS board contains up to 72 fibre-optic input links (grouped in 12-fibre MTP connectors) routed to general I/O pins. The readout links are 240 Mbps pseudo DC balanced following National Semiconductors DS90LV1021 protocol. Specific deserialization has been implemented to ensure reliable data reception.

The first batch of TwinMux boards has already been fabricated, was installed during 2015 technical stop, and is currently in production. One of these boards is used for a test stand for the uROS production and it is installed in CMS and connected to input links coming from the inner detector which have been optically splitted.

In this work we will detail the design of the uROS board and report the results from the first validation tests.

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