Digital Readout Board for CMS and TOTEM Precision Proton Spectrometer timing upgrade project

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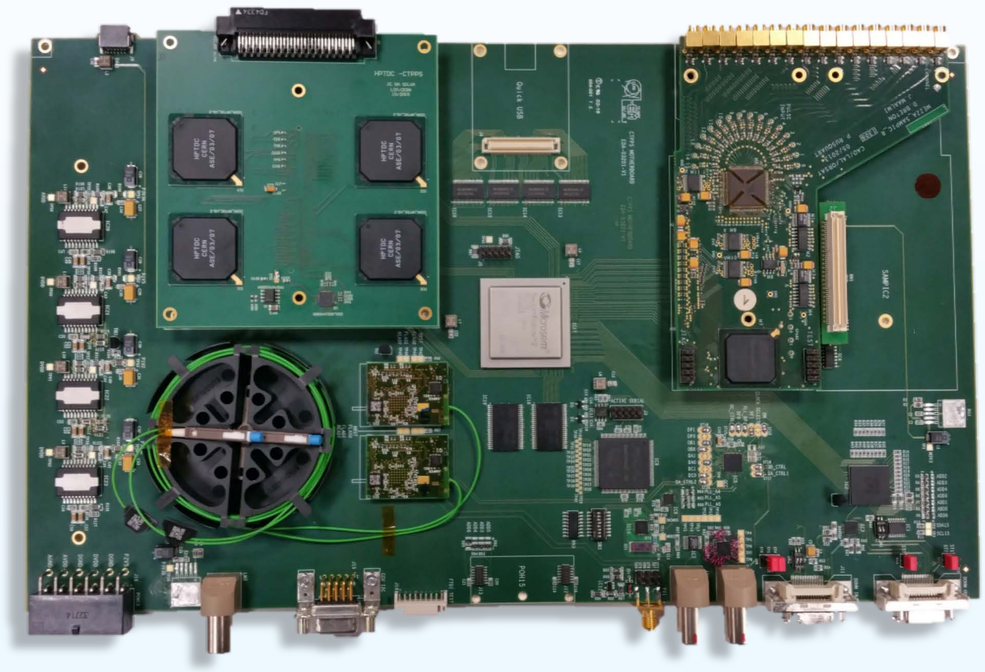
on behalf of CT-PPS collaboration

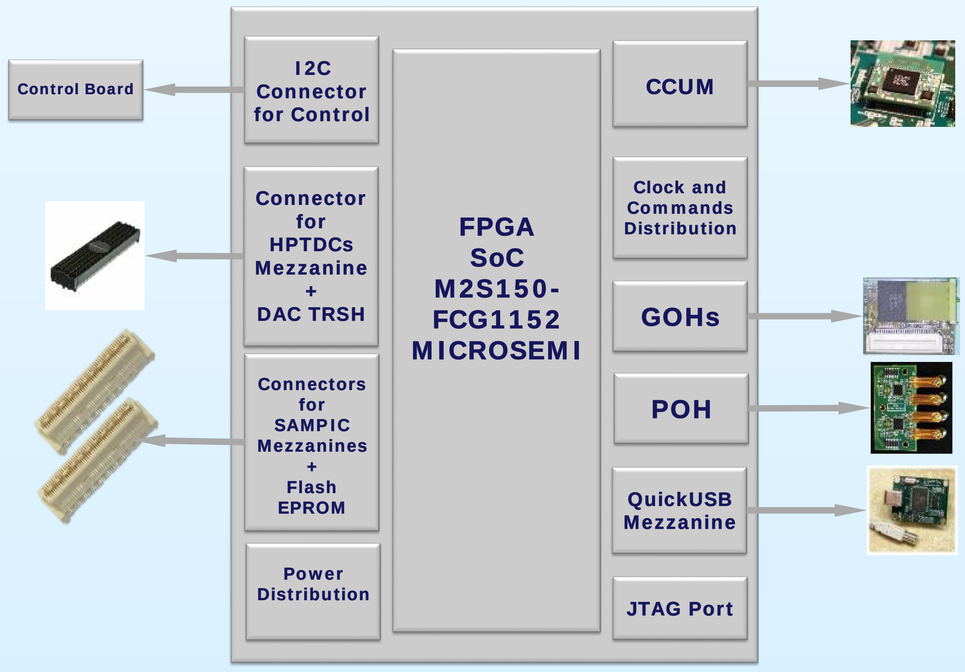
Introduction

For the CMS[1] and TOTEM[2] experiments Precision Proton Spectrometer (CT-PPS) project, a Digital Readout Board was designed to take front-end data of the Timing Detectors, reformat the data timing packets, and transmit them to the CMS and TOTEM data acquisition systems through optical data links. This board is capable of having HPTDC or SAMPIC mezzanines for high-resolution timing measurement of the leading and trailing edges in the hit pulses with the resolution of 10 - 20 ps.



Block Diagram

The Digital Readout Board is the main component of the CT-PPS Timing electronic system.



The main objectives of the board are to acquire on-detector data and trigger from the hybrids, to perform data conversion from electrical to optical format and to transfer it to the next level of the system. It also distributes the control information to the hybrids and collects different detector and board parameters.

Components

Control Logic Block – based on CCUM mezzanine. This module is connected to the control loop via two 20pins 3M high speed connectors placed on the front panel. Control logic block provides 16 I2C interface channels and one 8 bit parallel control port;

Clock and Commands Distribution Block – based on PLL25 chip, QPLL and a number of clocks and commands distribution circuitry. It delivers synchronous clock and commands to every component on the board including the FPGA on board;

FPGA and Data Transfer Block – based on rad-hard FPGA SmartFusion2 M2S150-FC1152 from Microsemi Co. Data transfer via GOH or POH modules at up to 400 Mb/sec.

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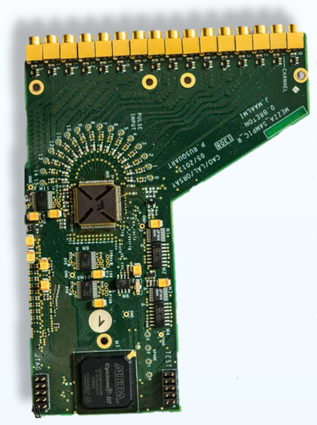
Mezzanines

The Digital Readout Board accepts several mezzanine modules:

HPTDC – based on four HPTDC chips on the board which forms a token ring controlled by the SmartFusion2 FPGA on the readout board. Specially designed front-end board with four NINO chips 8 channels each is connected to the inputs of the HPTDC mezzanine;

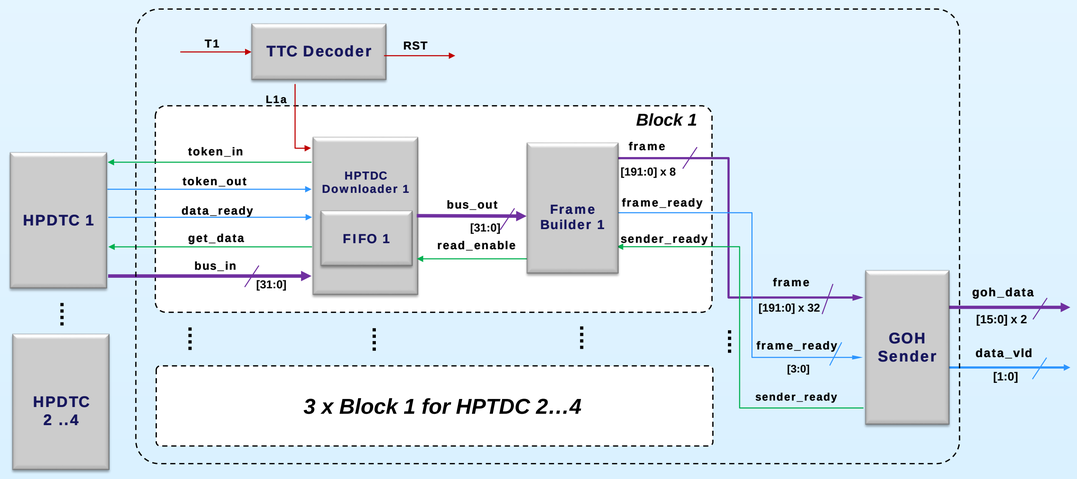


SAMPIC –The SAMPIC has 16 input channels with a sampling rate up to 10 Gs/s. Each channel works in a independent self-triggered mode and up to 64 sample can be acquired on each trigger. Such solution permits to sample the whole leading edge of the signal (~2 ns), allowing advanced offline reconstruction algorithms;

QuickUSB – for test purposes, USB and FieldBus expansions are also implemented on the board.

Firmware

The firmware has been built with Libero SoC 11.7 tools as hierarchical structure using VHDL and Verilog. Equivalent basic blocks are implemented for the 4 HPTDC mezzanines. The other parts of the design are under development.

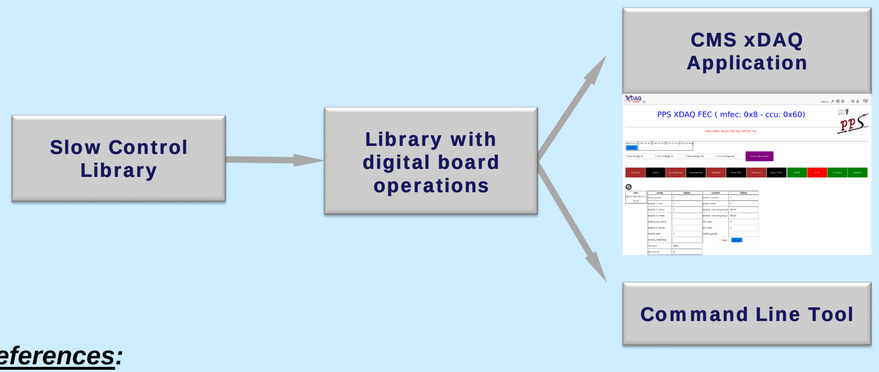


Software

The software[3] has been built on C++ and uses the CMS tracker slow control library. It realizes read/write operations on I2C buses, read/write data transparently from/to HPTDC using a bit ordering API, checks for transmission errors, transmit/receive FIFO information (µTCA or VME), handle errors and controls all the connected devices.

Command Line Tool – for debugging purposes.

CMS xDAQ Application – web interface software which controls the detector FSM and access to the Digital Readout Board devices.



References:
[1] "The CMS Experiment"
[2] "The TOTEM Experiment at the CERN Large Hadron Collider"
[3] Website: https://twiki.cern.ch/twiki/bin/viewauth/CMS/PpsFecSoftware